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Datasheet for the decision of 13 November 2017

Case Number: T 0013/13 - 3.5.02

Application Number: 05725604.2

Publication Number: 1751867

IPC: H03L7/189, H03J7/06, H03L7/099

Language of the proceedings: EN

Title of invention:
Adjustable frequency delay-locked loop

Applicant:
Motorola Solutions, Inc.

Relevant legal provisions:
EPC Art. 54, 56

Keyword:
Novelty - non-prejudicial disclosure
Inventive step - non-obvious solution

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Case Number: T 0013/13 - 3.5.02

D E C I S I O N
of Technical Board of Appeal 3.5.02
of 13 November 2017

Appellant: (Applicant)	Motorola Solutions, Inc. 500 W. Monroe Street 43rd Floor Chicago, IL 60661 (US)
Representative:	Treleven, Colin Optimus Patents Limited Peak Hill House Steventon Basingstoke, Hampshire RG25 3AZ (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 25 July 2012 refusing European patent application No. 05725604.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	R. Lord
Members:	M. Léouffre
	J. Hoppe

Summary of Facts and Submissions

I. On 25 September 2012 the applicant appealed against the decision of the examining division to refuse the European patent application No. 05 725 604.2, and requested that the contested decision be set aside and a patent be granted on the basis of the main request filed on 25 May 2012 or if that was not possible, on the basis of the auxiliary request filed on 20 June 2012.

II. The examining division held that the subject-matter of claims 1 to 7 and 9 of the main and auxiliary requests was not novel having regard to document US 2003/0099321 A1 (D1) while the subject-matter of claim 8 lacked an inventive step in the light of D1. The examining division also objected that claims 1, 3, 6, 8 and 9 of the main request and claims 1 and 9 of the auxiliary request lacked clarity (Article 84 EPC).

III. In its grounds of appeal the appellant announced its willingness to remove some of the objected wording for clarity reasons if necessary. On 20 October 2017, in response to a phone call from the rapporteur of the board, the appellant replaced the set of claims of the main request with a new set of claims 1 to 9 amended for improved clarity by deleting the wording "substantially" in the set of claims where it appeared and by adding the word "tap" in claim 7.

IV. Claim 1 of the main request reads as follows:

"A delay-locked loop (300) comprising:

an adjustable frequency source (320) for generating a clock signal (322) having an adjustable frequency;

an adjustment and tap selection controller (310) coupled to the adjustable frequency source (320) for:
(i) determining a first frequency ($F_{clkvariable}$) as a function of a desired output frequency (F_{out}), the number (N) of taps, and a range (F_{min}-F_{max}) of possible frequency values for the first frequency, the desired output frequency being the desired frequency of a first output signal (372);
(ii) causing a second period, corresponding to the desired output frequency (F_{out}), to be an integer multiple (M) of a delay, the delay being a first period corresponding to the first frequency ($F_{clkvariable}$) divided by the number of taps (N); and
(iii) causing said adjustable frequency source (320) to adjust the frequency of said clock signal (322) to said first frequency ($F_{clkvariable}$);

a delay line (330) configured to receive the clock signal (322) for generating a plurality of phase-shifted clock signals, each phase-shifted clock signal having said first frequency ($F_{clkvariable}$) and being shifted in phase with respect to the clock signal (322) and with respect to the other phase-shifted clock signals; and

a first selection circuit (370) for receiving the plurality of phase-shifted clock signals and for selecting, one at a time and under the control of the adjustment and tap selection controller (310), a first sequence of the phase-shifted clock signals for generating said first output signal (372) having said desired output frequency (F_{out})."

Claims 2 to 8 are dependent on claim 1.

Claim 9 reads as follows:

"A method for use in a delay locked loop (300), said method comprising the steps of:

determining (410) a first frequency ($F_{clkvariable}$) as a function of a desired output frequency (F_{out}), the number (N) of taps, and a range (F_{min}-F_{max}) of possible frequency values for the first frequency, the desired output frequency being the desired frequency of a first output signal (372); causing a second period, corresponding to the desired output frequency (F_{out}), to be an integer multiple (M) of a delay, the delay being a first period corresponding to the first frequency ($F_{clkvariable}$) divided by the number of taps (N); and

outputting (430) at least one frequency adjustment value for causing a clock signal (322) to be generated having said first frequency and for further causing a plurality of phase-shifted clock signals to be generated, each phase-shifted clock signal having said first frequency and being shifted in phase with respect to the clock signal and with respect to the other phase shifted clock signals;

determining (420) a first sequence of selection values corresponding to a first sequence of the plurality of phase-shifted clock signals; and

outputting (450) said first sequence of selection values for causing said first sequence of phase-shifted clock signals to be selected one at a time for generating said first output signal (372) having said desired output frequency (F_{out})."

V. The appellant argued essentially as follows:

The Guidelines F-IV 4.2 specified the approach to clarity that the examining division should follow and pointed out that: "Each claim should be read giving the words the meaning and scope which they normally have in the relevant art", and "The claim should also be read with an attempt to make technical sense out of it."

At point II, 2.2 of the decision the examining division discussed the signal 254 output by multiplexer 250 in the upper centre of FIG. 8 of D1. The final four lines of point II, 2.2 of the decision stated that: "The instantaneous frequency of (254) i.e. the instantaneous "first frequency" in this example is thus either F_{ref} (for 7 periods) or 32/(32+8) * F_{ref} (for 1 period). The average frequency of (254) i.e. the average "first frequency" is 32/(32+1) * F_{ref} = F_{out}".
The division demonstrated here that signal 254 switched regularly between two different values. However a signal that dropped in frequency by 20% for 1/8 of the time would not be an acceptable clock signal.
Therefore, under no circumstances would a skilled person have believed that signal 254 was a clock signal, in the sense of that of claim 1 of the present application. On the contrary the "first frequency" in claim 1 of the application was just one frequency, as was normal for a clock signal. The applicant pointed out in great detail in the written submission dated 25 May 2012 why the division was incorrect. The examining division did not address this argument and committed therefore a procedural violation similar to the one recognised in case T1442/09 of November 2010.

In contrast to D1, the invention required a variable input clock and a means of controlling the adjustable frequency source and tap selection to force the period of the output signal to be an integer number M of delays (T_{clk}/N), T_{clk} being the period of the adjustable frequency source. This resulted in the quantized edge transition times of the actual output signal corresponding with the desired edge transition times to reduce and ideally eliminate spurious signals in the output, as recited at page 6, lines 13 to 17 of the international application as originally filed (WO 2005/109647 A2).

D1 used a primary delay line element 24 and a secondary delay line element 310 to increase the resolution of the primary delay line (see for example the abstract of D1). Paragraph [0054] of D1 stated that "Taps are then sequentially selected to produce an output at time increments approximating K.C times the reference clock period." The key word in this description was "approximating". Thus, while D1 used finer delay elements to improve the spurious performance of its output signal (providing a better approximation of the desired output frequency), the spurious free dynamic range of D1 was still, in general, limited by the quantization effects of the taps. In contrast, the invention of claim 1 of the present application controlled the "adjustable frequency input and tap selection" to force the period of the desired output signal to be an integer number M of delays T_{clk}/N, which greatly improved the spurious free dynamic range of the output. This provided sufficient improvement to meet the output spurious requirements for some hand-held communication devices.

D1 did not force an integer relationship between the delay values T_{clk}/N and the period of the output signal. Instead, D1 used more finely quantized delays, to try to reduce the error which caused spurious signals. Considering the practical case of the need to provide a frequency source for a band of radio frequency communication channels with a certain channel spacing, even if D1 were chosen to provide these frequencies, D1 would not have provided the integer relationship discussed above for these frequencies, in order to meet both frequency and spurious signal requirements.

The features and function of claim 1 of the main request of the present application did provide this integer relationship, and therefore vastly improved spurious performance over the prior art approaches, such as that in D1. A comparison of figures 2 and 7 of the present application demonstrated this.

It would not have been obvious for the person skilled in the art to adapt the arrangement of D1 to show the limitations of claim 1 of the main request. The skilled person would not have seen the possibility of constraining the first frequency $F_{Clkvariable}$ as specified in points (i) and (ii) of claim 1, given the complexity of the constraints on N, M and F_{min}-F_{max} specified there. Only such constraints led the invention to provide the spurious signal performance that was shown in figure 7 of the application, cf. also figure 2 of D1.

The DLL of the present invention was designed to provide the frequency generation needed for radio products, particularly multi-band two-way radios. Such products had challenging performance specifications,

and hence needed great stability in the signals that they generated. The invention was created out of a need to meet spurious requirements, with a DLL type of frequency generation scheme.

The DLL of D1 was designed to improve frequency resolution (see paragraph [0075] of D1). However, the quantized nature of the DLL of D1 would not have met the stringent requirements for spurious signals, which radio products faced. Thus the skilled person would not have turned to D1, when seeking to address the problem solved by the present invention (see on this point page 4, lines 11 to 19 and figure 2 of the present application). Figure 2 of D1 showed exactly the quantization errors that the text in page 4, lines 11 to 19 of the present application described as being problematic.

The invention adjusted the input variable frequency source 320 and tap selection so that there was an integer relationship between delay times and the output signal period. D1 did not have the constraints specified in point (i) of claim 1 of the main request, so did not anticipate claim 1. Even arriving at a given signal in D1 by coincidence, by different means to those in claim 1 of the main request, did not anticipate the means specified in claim 1 of the main request, and nor did it render the means of claim 1 obvious.

Concerning the clarity objections raised by the examining division under point II, 5.1 of the decision, the applicant removed the word "substantially" from the claims.

Concerning point II, 5.2 of the decision, the range F_{min}-F_{max} of point (i) of claim 1 of the main request was explained in the originally filed international application from page 9, line 10 to page 11, line 15. F_{min}-F_{max} was an additional constraint, within the usual frequency limitations of an adjustable frequency source. No greater detail was required in claim 1 than the fact that such a constraint existed. Following the Guidelines F-IV 4.5.3, "It is not necessary to include all the details of the invention in the independent claim". The mere fact that a limit (F_{min}-F_{max}) was stated in claim 1 indicated that this was a feature other than the intrinsic performance boundaries of the adjustable frequency source.

Concerning point II, 5.3 of the decision, a delay-locked loop of the kind shown in the application had taps. It was therefore reasonable to refer to them as "the taps".

Concerning point II, 5.4 of the decision, the first line of point (ii) of claim 1 referred clearly to a second period, corresponding to the desired output frequency F_{out}. It was absolutely clear what this phrase meant. An output frequency had a period, and this did not need to be specified further.

Reasons for the Decision

1. The appeal is admissible.

2. The appellant alleged that the examining division committed a substantial procedural violation by not addressing the applicant's argument raised in the written submission dated 25 May 2012, namely that the variable signal 254 at the output of the multiplexer

250 shown in figure 8 of D1 was not to be considered as clock signal.
The examining division did however explicitly address this argument in the reasons for the decision under item II.2.4. That the examining division did not share the appellant's opinion about the the variable signal 254 does not constitute a substantial procedural violation but reveals a difference of opinion. Furthermore, considering the estimation done by the examining division of the frequency values of the signals 254 and 350 output by the multiplexers 250 and 310 shown in figure 8 of D1 (see item II.2.6 of the reasons for the decision), which is shared by the board (see item 5 below), there is no need to decide whether the signal 254 of D1 is a clock signal or not.

3. Article 84 EPC

3.1 The examining division objected that the term "substantially" was vague and rendered the subsequent features of claim 1 unclear. The term "substantially" has now been removed from all the claims where it appeared previously.

3.2 The examining division objected that "It is unclear what restriction - if any - the phrase "a range of possible frequency values for the first frequency" is intended to add to claims 1 and 9, as the first frequency can only be determined to be a frequency value within a range which is possible, and not - by definition - a frequency value within a range which is impossible" (see item II, 5.2 of the reasons for the decision).

According to claim 1 the controller 310 determines a relation between the desired output frequency, i.e a

known frequency value F_{out}, and a first frequency F, which is unknown, taking account of the number N of taps. The example given in the description is $F=(F_{out}/N)*M$ (see equation 5 at page 9 of the published description) whereby M would be an integer. Thus M can only be determined if a range of values for the frequency F is taken in account. Therefore the range is correctly mentioned and necessary for the definition of the invention as claimed in claim 1.

3.3 Concerning the feature "the number of taps" (item II, 5.3 of the reasons for the decision), it is notorious that a delay locked loop as claimed in claim 1 or mentioned in the method claim 9 is provided with a certain number of taps. Hence the feature "the number of taps" refers implicitly to the taps of the delay locked loop, and a person skilled in the art willing to understand would have interpreted the claim in the sense that the feature "the number of taps" refers to the total number of taps of the delay-locked loop. Reading the claim in the context of the application, the skilled person would not have interpreted the number of taps as a number of selected taps as suggested by the examining division because neither claims 1 and 9 nor the whole disclosure of the patent application consider a particular number of selected taps as suggested by the examining division.

3.4 The examining division objected that the nature of the correspondence between the second period and the desired output frequency and that between the first period and the first frequency were not specified, and that there was no one to one correspondence (item II, 5.5 of the reasons for the decision).
This objection is understood to relate to feature (ii) of claim 1 (and the similar feature in claim 9) which

solely mentions "a second period, corresponding to the desired output frequency (F_{out})" and "the delay being a first period corresponding to the first frequency ($F_{clkvariable}$)".
Even if it is admitted that, semantically, the term "corresponding" may imply any kind of relation between two values, a skilled person knows that the frequency of a signal always corresponds to a period which is the inverse of that frequency. Hence, in the context of the application, a person skilled in the art with a mind willing to understand would have interpreted the term "period" mentioned in each of these two features as defining the inverse of each of the first and desired output frequencies.

3.5 The examining division objected also that in claims 1 and 9 no use was made of "the second period" once it has been caused and that what the second period is was not specified (item II, 5.4 of the reasons for the decision).

As indicated under item 2.4 above, a person skilled in the art would have understood the expression "a second period, corresponding to the desired output frequency (F_{out})" found in feature (ii) of claim 1 as the period of the signal having the desired output frequency.
Thus, after having determined the first frequency and implicitly a possible integer as mentioned under item 2.2 above, the controller 320 adjusts the frequency of the clock signal to the determined first frequency and causes a second period which is the period of the output frequency to be multiplied by the integer which has been implicitly determined together with the first frequency.
Hence a person skilled in the art with a mind willing to understand would have understood that the integer M

is implicitly determined together with the first frequency, that the features indexed with (ii) and (iii) in claim 1 should not be interpreted as defining chronological steps, and that the second period means nothing else than the period of the signal output by the delay locked loop.

3.6 The above comments apply equally to claim 9.

3.7 For the reasons indicated above the claims 1 and 9 are considered as satisfying the requirements following from Article 84 EPC.

4. Article 123(2) EPC

New claim 1 is based on original claim 1 wherein the feature "an adjustment tap and selection controller for determining a first frequency as a function of a second frequency and for causing said frequency source to adjust the frequency of the clock signal to substantially said first frequency, said second frequency being the desired frequency of a first output signal" has been replaced by the features (i) and (iii), in which the term "substantially" has been suppressed and the "second frequency" has been renamed "desired output frequency".

The removal of the term "substantially" clarifies the subsequent features and thereby limits the scope of the claims. The description of the original published international application in the last paragraphs of pages 6 and 12 recites that the delay-locked loop takes account of the range of possible frequency values and the number of taps N, so that the features (i) and (iii) do not extend the scope of the claims beyond the content of the original application.

Feature (ii) has also been added to claim 1. Feature (ii) defines the relation between the period of the first frequency and the period of the desired output frequency, which is the usual relation established when the frequency of the clock signal is adjusted according to the invention, i.e. the ideal case defined by equation 5 at page 9 of the original application. Hence, claims 1 and 9 do not contravene Article 123(2) EPC.

5. Article 54 EPC

5.1 Under items II, 2.2 and II, 2.3 of the contested decision the examining division referred to figure 8 of document D1 and considered the signal 254 at the output of the multiplexer 250 as corresponding to the first frequency and the signal 350 at the output of the multiplexer 344 as representing the second frequency specified in the present claim 1, i.e. the desired frequency of the output signal (see lines 5 and 14 on page 4 of the contested decision).

The examining division based their reasoning on a particular example having 32 taps, whereby N=4 and M=8 and "the sequence advances by one delay unit of the fine delay line 310 every period of the reference clock" (see item II, 2.2 of the reasons for the decision).

While the values 4 and 8 for N and M are disclosed in D1 (see paragraph [0104]), the particular case wherein "the sequence advances by one delay unit of the fine delay line 310 every period of the reference clock" is not disclosed.

Thus it cannot be concluded that the subject-matter of claim 1 is known from D1.

5.2 This particular example also does not deprive the subject-matter of claims 1 and 9 of novelty for the following reasons:

On the basis of the example taken by the examining division, the board agrees that the instantaneous frequency of signal 254, i.e the instantaneous "first frequency" in this example, is an average of frequency F_{ref} for 7 periods and $1/(T_{ref} + T_{ref}/4)$, in other words $(32/(32+8))*F_{ref}$ for one further period, T_{ref} and F_{ref} being the period and frequency of the reference clock at input 48 in figure 8. Thus, the average frequency of signal 254 i.e. the average "first frequency" equals indeed $(32/(32+1))*F_{ref}$.

It follows from this that the first frequency equals the second frequency which is the output frequency F_{out} of signal 350 as admitted by the examining division at page 4, lines 6, 16 and 17 of the decision.
Hence the delay line behaves in this particular case as if there were a single delay line having 32 taps.

From the above, an integer M may be considered which has a value of 32+1. However M does not characterise a ratio between the first and second frequencies as defined by the examining division, but a ratio between the frequency at the output 350 of multiplexer 344 or multiplexer 250 and the reference clock.
Thus, the frequency of the reference clock of D1 is not determined as a function of a desired output frequency, the number of taps and a range of possible frequency values for the first frequency, and there is in D1 no frequency adjustment value for causing a clock signal

to be generated having substantially the first frequency.
The subject-matter of the present claims 1 and 9 is therefore novel having regard to D1.

6. *Article 56 EPC*

According to the prior art cited above, M being an integer results from the choice of the example whereby the sequence advances by one delay unit of the fine delay every period, the ratio between the the clock or reference frequency and the output frequency and F_{ref}/ F_{out} being equal to K.C , K being an integer and C representing a decimal, and C or C/K being proportional to 1/32 or 1/N, N being the number of taps (see D1, paragraphs [0040] and [0041]) as acknowledged by the examining division at page 4, line 1 of the grounds for the decision.

This corresponds to an ideal situation where there is no misalignment between the desired output signal transitions and the real and possible output signal transitions, as shown in figure 2 of the application and discussed in the application at pages 2 and 3.

For producing other desired output frequencies in D1, other sequences of taps could be needed which would only allow to produce an output signal approximating the desired frequency. These tap sequences would lead to misalignments between the instants of the output signal and the instants of the desired output signal transitions corresponding to the desired frequency, and would produce spurious signals. The invention allows for a certain range of frequencies F_{min}-F_{max} of the clock signal to match the instants of transition of the output signal to the transition instants of the desired

output signal. In other words the problem of the present application disclosed in relation to figures 1 to 3 of the application is not addressed, let alone solved by D1.

The subject-matter of claim 1 is therefore considered as not obvious having regard to the available prior art (Article 56 EPC).

7. For the above reasons, all of the objections raised by the examining division have either been determined to be invalid or have been overcome by amendment, and the board is not aware of any further objections. The appellant's request therefore meets the requirements of the EPC and thus provides a basis for grant of a patent.

Order

For these reasons it is decided that:

1. The contested decision is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:
Description:
Pages 1 to 4 and 6 to 19 as published
Pages 5, 5a and 20 filed with telefax on 15 May 2011
Claims: No. 1 to 9 filed with the letter dated 20 October 2017
Drawing sheets:
1/6 to 6/6 as published

The Registrar: The Chairman:

U. Bultmann R. Lord

Decision electronically authenticated

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Case Number: T 0013/13 - 3.5.02

D E C I S I O N
of Technical Board of Appeal 3.5.02
of 25 January 2018 correcting an error in the decision

of 13 November 2017

Appellant: (Applicant)	Motorola Solutions, Inc. 500 W. Monroe Street 43rd Floor Chicago, IL 60661 (US)
Representative:	Treleven, Colin Optimus Patents Limited Peak Hill House Steventon Basingstoke, Hampshire RG25 3AZ (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 25 July 2012 refusing European patent application No. 05725604.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	R. Lord
Members:	M. Léouffre
	J. Hoppe

In application of Rule 140 EPC, the decision of the Technical Board of Appeal given on 13 November 2017 is hereby corrected as follows:

on page 17, point 2., **Order**, the correct date of the filed telefax is 13 May 2011.

The order thus reads:

For these reasons it is decided that:

1. The contested decision is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:
   Description:
   Pages 1 to 4 and 6 to 19 as published
   Pages 5, 5a and 20 filed with telefax on 13 May 2011
   Claims: No. 1 to 9 filed with the letter dated 20 October 2017
   Drawing sheets:
   1/6 to 6/6 as published

The Registrar: The Chairman

U. Bultmann R. Lord

Decision electronically authenticated