Internal distribution code:

(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 28 August 2017

Case Number: T 1987/12 - 3.5.06

Application Number: 03748384.9

Publication Number: 1554647

IPC: G06F9/38, G06F1/32, G06F9/30

Language of the proceedings: EN

Title of invention:
VLIW PROCESSOR WITH POWER SAVING

Applicant:
Intel Corporation

Headword:
VLIW power saving/INTEL

Relevant legal provisions:
EPC 1973 Art. 56

Keyword:
Inventive step - (yes)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 1987/12 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 28 August 2017

Appellant: (Applicant)	Intel Corporation 2200 Mission College Boulevard Santa Clara, CA 95054 (US)
Representative:	V.O. P.O. Box 87930 2508 DH Den Haag (NL)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 17 April 2012 refusing European patent application No. 03748384.9 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	W. Sekretaruk
Members:	G. Zucka
	A. Teale

Summary of Facts and Submissions

I. The appeal is against the decision by the examining division, dispatched with reasons on 17 April 2012, to refuse European patent application 03748384.9, on the basis that the subject-matter of independent claim 1 of the main and the auxiliary request was not inventive, Article 56 EPC 1973, and independent claim 6 of the main request was not supported by the description, Article 84 EPC 1973. The following documents were referred to in the reasons for the decision:

D1 = US 6 219 796 B1
D2 = US 6 026 479 A

II. A notice of appeal was received on 15 June 2012, the appeal fee being paid on the same day. A statement of grounds of appeal was received on 20 August 2012.

III. The appellant requested that the decision under appeal be set aside and a patent granted on the basis of the claims of a main or one of three auxiliary requests, all filed with the grounds of appeal. The appellant made a conditional request for oral proceedings.

IV. The board issued a communication setting out its preliminary opinion, according to which the main request and auxiliary request 1 did not satisfy the requirements of Article 84 EPC 1973.

V. On 7 August 2017, the appellant filed a new main request and new auxiliary requests 1 to 3.

VI. The appellant requests that the decision under appeal be set aside and a patent be granted on the basis of claims 1 to 6 of the main or first auxiliary request, or claims 1 to 5 of the second or third auxiliary request, all filed with the letter of 7 August 2017.

The further text on file for all requests is:

Description
Pages 1, 4 and 6 to 7 as originally filed,
Pages 2, 2a, 3, 3a, 5 and 5a as filed with the grounds of appeal;

Drawings
Sheet 1 as filed with the grounds of appeal.

VII. Independent claim 1 of the main request reads as follows:

"A data processing apparatus, the apparatus comprising
- an instruction memory system arranged to output an instruction word, capable of containing a plurality of instructions, respective instruction words being output in response to respective instruction addresses;
- an instruction execution unit, comprising a plurality of functional units, each capable of executing a respective instruction from the instruction word in parallel with execution of other instructions from the instruction word by other ones of the functional units;
- a power saving circuit arranged to switch a selectable subset of the functional units and/or parts of the instruction memory that supply instructions from the instruction word to the functional units to a power saving state during program execution, the power saving circuit being arranged to select the functional units

and/or parts of the instruction memory in the subset dependent on program execution,
characterized in that the power saving circuit is arranged to select the subset dependent on an instruction address in response to which the instruction memory system outputs the instruction word."

VIII. The other independent claim, *i.e.* claim 6, of the main request reads as follows:

"A method of executing a program of instructions using a data processing apparatus according to claim 1, the method comprising a step before execution of identifying combinations of (groups of) functional units that are used in respective sections of the program and compiling information that indicates which combinations are used in which sections, and subsequently during execution, using the compiled information to disable clock signals selectively in those (groups of) functional units that are not used in a section when instructions from the section are executed."

Reasons for the Decision

1. *The admissibility of the appeal*

The appeal is admissible.

2. *Main request - clarity, support by the description and essential features; Article 84 EPC 1973*

2.1 The board is satisfied that the preliminary objections under Article 84 EPC 1973 which it had raised in its communication have been overcome by the amendments to claims 1 and 6 of the main request.

2.2 According to the appealed decision (Reasons 18.2), it was doubtful whether claim 1 comprised all features essential for the performance of the invention, given that the claimed apparatus lacked means to identify which combinations of (groups of) functional units were used in which program sections.

The board is of the opinion that it follows from the inventive step reasoning given below that the identification means are not an essential part of the invention.

2.3 As regards the use of parentheses in line 15 of claim 6, the board holds that the expression "combinations of (groups of) functional units" is unambiguous and has the same meaning as "combinations of functional units or groups of functional units".

3. *Main request - inventive step; Article 56 EPC 1973*

3.1 The board considers that D1 forms the closest prior art. As stated in the appealed decision (point 14.1) and as agreed by the appellant, the difference between the apparatus of claim 1 and the disclosure of D1 is that the power saving circuit is adapted to select the subset of functional units and/or parts of the instruction memory to a power saving state dependent on

an instruction address in response to which the instruction memory system outputs the instruction word.

As described on page 7, lines 25 to 31 of the description, the instruction address dependency would typically be determined by memory mapping information indicating which combinations of (groups of) functional units are used in respective sections of the program.

3.2 In this way, it is not necessary to use specific instructions which control the power mode of the processor.

3.3 The board agrees with the appealed decision (Reasons, point 15) that, apart from switching ILP modes by means of dedicated switching instructions in the program, D2 discloses an alternative according to which the ILP mode may be switched following an interrupt signal received by the CPU (see D2, column 6, lines 8 to 47). This fact was not denied by the appellant.

The board agrees with the appellant (grounds of appeal, point I.4.2, third to penultimate paragraph), in contrast with the assessment made in the appealed decision (Reasons, point 15), that there is no indication in D2 that the interrupts could be generated by the user in order to switch the ILP mode at certain instruction addresses. The interrupt signals in D2 result in the calling of diverse interrupt *routines* (which would happen to be either low or high ILP mode routines). These interrupts are therefore clearly not *intended* merely to switch the ILP mode but simply may or may not, depending on the interrupt routine, result in a change of ILP mode.

It is not apparent from any passage in D2 that the use of interrupts, let alone user-generated interrupts, in itself would provide some inherent advantage over the use of program instructions that explicitly switch functional units to a power saving state. It is rather apparent that the only reason why D2 describes a specific procedure for dealing with interrupts is that such interrupts may happen at any time during program execution, *i.e. not* at specific instruction addresses where it would be possible to insert ILP mode switching instructions.

The skilled person would have had therefore no incentive to combine the teaching of D1 and D2 and thereby arrive at the subject-matter of claim 1.

3.4 The subject-matter of claim 1 of the main request is therefore considered inventive; Article 56 EPC 1973.

3.5 The subject-matter of claim 6 of the main request, which relates to a method using the apparatus of claim 1, is also considered inventive.

Order

For these reasons it is decided that:

1. The appealed decision is set aside.
2. The case is remitted to the department of first instance, with the order to grant a patent on the basis of the appellant's main request referred to under VI. above.

The Registrar: The Chairman:

B. Atienza Vivancos W. Sekretaruk

Decision electronically authenticated