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Datasheet for the decision of 20 March 2015

Case Number: T 1542/12 - 3.5.05

Application Number: 05011018.8

Publication Number: 1564949

IPC: H04L25/02, H04L25/10

Language of the proceedings: EN

Title of invention:
Reduction of common mode signals

Applicant:
FUJITSU LIMITED

Headword:
Receiver circuit/FUJITSU

Relevant legal provisions:
EPC Art. 83
RPBA Art. 13(1), 13(3)

Keyword:
Sufficiency of disclosure - (no)
Admission of late-filed request - (yes)

Decisions cited:

Catchword:

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Case Number: T 1542/12 - 3.5.05

D E C I S I O N
of Technical Board of Appeal 3.5.05
of 20 March 2015

Appellant: (Applicant)	FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku Kawasaki-shi, Kanagawa 211-8588 (JP)
Representative:	Stebbing, Timothy Charles Haseltine Lake LLP Lincoln House, 5th Floor 300 High Holborn London WC1V 7JH (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 15 February 2012 refusing European patent application No. 05011018.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	A. Ritzka
Members:	K. Bengi-Akyuerek
	D. Prietzel-Funk

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division, posted on 15 February 2012, to refuse European patent application No. 05011018.8 on the grounds of lack of inventive step (Article 56 EPC) with respect to a main request and first to fourth auxiliary requests, mainly having regard to the disclosure of

D1: US-A-4 697 152.

In an *obiter dictum* under the heading "Further Remarks", the examining division expressed its doubts about the compliance of the claims of the main request and first to third auxiliary requests with Articles 84 and 83 EPC.

II. Notice of appeal was received on 12 April 2012. The appeal fee was paid on the same day. With the statement setting out the grounds of appeal, received on 18 June 2012, the appellant filed new claims according to a main request and two auxiliary requests. It requested that the decision of the examining division be set aside and that a patent be granted on the basis of the main request or either of the auxiliary requests.

III. A summons to oral proceedings scheduled for 20 March 2015 was issued on 22 December 2014. In an annex to this summons, the board gave its preliminary opinion on the appeal pursuant to Article 15(1) RPBA. In particular, it raised objections under Article 123(2) EPC and provided a preliminary opinion on novelty and inventive step, having regard to D1.

IV. With a letter of reply dated 19 February 2015, the appellant submitted amended claims according to a new

main request and new first and second auxiliary requests.

V. Oral proceedings were held as scheduled on 20 March 2015. During the oral proceedings the appellant submitted a new set of claims as a new request in response to objections raised by the board under Article 123(2) EPC during the oral proceedings, and withdrew all the other requests on file. The new request was admitted into the appeal proceedings and was discussed.

The appellant's final request was that the decision under appeal be set aside and that a patent be granted on the basis of the new request filed at the oral proceedings before the board.

At the end of the oral proceedings, the decision of the board was announced.

VI. Claim 1 of the new request (sole request) reads as follows:

"A receiver circuit comprising:

a capacitor network (2001) for receiving differential input signals via a plurality of input terminals (V+, V-), having a plurality of capacitors, and a plurality of switches connected between said capacitors and the input terminals (V+, V-) for reducing a common-mode voltage contained in the differential input signals in a low-frequency range;

a comparator (2002) consisting of inverters (2021, 2022) for amplifying the outputs of said capacitor network (2001) and a common-mode feedback circuit (2003) for receiving the outputs of said inverters, said common-mode feedback circuit (2003)

including a detector (2031) which is a differential amplifier having two pairs of input transistors, said detector (2031) providing a sum of the outputs of said inverters (2021, 2022) corresponding to a common-mode voltage remaining in the outputs of said capacitor network, and a feedback unit (2032) for carrying out a feedback operation to further reduce a common-mode voltage contained in the differential input signals in a high-frequency range;

a precharge circuit (2015, 2016) arranged at input terminals of said comparator (2002), said precharge circuit precharging said comparator (2002) by applying a predetermined source voltage to input terminals of said comparator; wherein

said capacitor network (2001) includes:

a first switch (2011) and a first capacitor (2017) connected in series between one (V+) of the input terminals and said first inverter (2021), and a second switch (2014) and a second capacitor (2018) connected in series between the other (V-) of the input terminals and said second inverter (2022), and

said capacitor network (2001) and said precharge circuit (2015, 2016) are operable in a first phase of accumulating voltages of the differential input signals and precharging the input terminals of said comparator (2002) and a second phase of supplying the outputs of said capacitor network to said comparator (2002), and to repeat the first and second phases to reduce the common-mode voltage contained in the differential input signals in said low-frequency range; and

said feedback unit (2032) includes two feedback transistors (2321, 2322) each arranged to receive said sum of the outputs of the inverters (2021, 2022) and

each having an output fed back to the output of a respective one of the inverters."

Reasons for the Decision

1. The appeal is admissible.

2. SOLE REQUEST

This request was submitted during the oral proceedings before the board, i.e. at a very late stage of the procedure. Nonetheless the board admitted it into the appeal proceedings under Article 13(1) and 13(3) RPBA, since it was regarded as a legitimate - though unsuccessful (see point 2.1 below) - attempt to overcome the objections raised by the board under Article 123(2) EPC, and since the board could deal with it without having to adjourn the oral proceedings.

Claim 1 of this request differs from claim 1 of the main request underlying the appealed decision essentially in that it now specifies that

A) the feedback unit carries out a feedback operation to <u>further reduce</u> a common-mode voltage contained in the differential input signals <u>in a high-frequency range</u> (emphasis added by the board) and that
B) said feedback unit includes two feedback transistors each arranged to receive said sum of the outputs of the inverters and each having an output fed back to the output of a respective one of the inverters.

Feature A) is supported e.g. by page 40, lines 16-24 of the application as filed. The board also accepts that feature B) finds its support in the teaching of page 40, lines 3-19 and Fig. 32 in conjunction with page 43, lines 12-14 and Fig. 38 of the original application, as provided by the appellant as a basis at the oral proceedings before the board.

2.1 Article 83 EPC

The board judges that claim 1 of this request does not meet the requirements of Article 83 EPC, for the following reasons:

2.1.1 The board first notes that, in respect of the requirements of Article 83 EPC, it has to be established whether the person skilled in the relevant art is enabled by the application together with his common general knowledge to put the claimed invention over the whole range claimed into practice, without undue burden. In this regard, the context of that application and its technical addressee has to be taken into account when assessing the enablement of the claimed invention. In the present case, the application is addressed to a person skilled in the field of signal transmission circuits (see e.g. page 1, first paragraph of the application as filed).

2.1.2 According to the proposed receiver circuit of the present invention, capacitor network 2001 is dedicated to reducing the common-mode voltage inherent in the differential input signals V+ and V- in a *low-frequency* range, whilst comparator 2002 is responsible for further reducing the resulting common-mode voltage (i.e. the common-mode voltage which has been already reduced to some extent in the low-frequency range by

the capacitor network) in a *high-frequency* range (cf. page 37, lines 2-6; page 38, lines 16-19; page 39, lines 10-14 and claim 2 of the application as originally filed). Moreover, a feedback unit, comprised in said comparator, is supposed to carry out a feedback operation to achieve the goal of further reducing the respective common-mode voltage included in the differential input signals (cf. page 40, lines 19-20 of the application as filed). To this end, according to feature B) of claim 1, said feedback unit includes two feedback transistors each arranged to receive said sum of the outputs of inverters 2021 and 2022 and each having an output fed back to the output of a respective one of the inverters (see also Fig. 32).

2.1.3 However, the board finds that the present application is completely silent as to a coherent and deterministic teaching about the implementation details of such a feedback process. From the original application, the skilled person in the field of signal transmission circuits would recognise at best that the output signals of the transistors of feedback unit 2032, such as PMOS transistors 2321 and 2322, are apparently connected to the respective outputs of inverters 2021 and/or 2022 via corresponding circuit nodes (see in particular page 40, lines 7-14 together with Fig. 32). Moreover, the skilled person would understand that those output signals constitute electrical currents. Accordingly, the skilled person would deduce from the above simply that some kind of feedback information in the form of a physical current is fed back to the inverters from which in turn some kind of output information in the form of a physical current is derived to be fed again into the feedback unit's transistors.

However, at least two issues regarding feature B) remain fully in the dark, namely (i) which *feedback information* the output signals associated with the outputs of the feedback unit's transistors are supposed to convey to the inverters and (ii) how the devised *feedback loop* is actually intended to be realised in order to indeed achieve the predefined goal of further reducing the common-mode voltage of the differential input signals of the receiver circuit under consideration. In particular, as to issue (i), the skilled person cannot derive any instructions from the original disclosure about whether e.g. the feedback data should convey the common-mode voltage detected or information about the level or extent to which the voltage reduction ought to be performed. As regards question (ii), the skilled person would be at a loss when trying to establish whether the corresponding common-mode voltage is to be compared with a predefined threshold level as, for example, proposed in D1 (see column 5, lines 12-24) or whether such a threshold is statically defined or dynamically adjusted, e.g. conditional on the signal frequency, or whether anything else is foreseen.

Neither could the appellant, at the oral proceedings before the board, provide any other disclosure of the present application, apart from the teachings relating to Figs. 32 and 38, which might lend additional support to resolve the aforementioned issues.

2.1.4 Therefore, the board concludes that the present invention as defined by claim 1 is not so clearly and completely disclosed that a skilled person could carry it out within the meaning of Article 83 EPC.

2.2 In conclusion, the sole request is not allowable under Article 83 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

K. Götz-Wein A. Ritzka

Decision electronically authenticated