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# Datasheet for the decision of 9 March 2017

**Case Number:** T 1425/12 - 3.5.06

**Application Number:** 06789683.7

**Publication Number:** 1913468

**IPC:** G06F9/30

**Language of the proceedings:** EN

**Title of invention:**
Method and system for providing an energy efficient register file

**Applicant:**
Qualcomm Incorporated

**Headword:**
Register file/QUALCOMM

**Relevant legal provisions:**
EPC 1973 Art. 56, 83

**Keyword:**
Sufficiency of disclosure - (yes)
Inventive step - after amendment (yes)

**Decisions cited:**

**Catchword:**

Europäisches Patentamt
European Patent Office
Office européen des brevets

**Beschwerdekammern**
**Boards of Appeal**
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**Case Number: T 1425/12 - 3.5.06**

# D E C I S I O N
# of Technical Board of Appeal 3.5.06
# of 9 March 2017

| | |
|---|---|
| **Appellant:** (Applicant) | Qualcomm Incorporated<br>5775 Morehouse Drive<br>San Diego, CA 92121 (US) |
| **Representative:** | Tomkins & Co<br>5 Dartmouth Road<br>Dublin 6 (IE) |
| **Decision under appeal:** | **Decision of the Examining Division of the European Patent Office posted on 12 December 2011 refusing European patent application No. 06789683.7 pursuant to Article 97(2) EPC.** |

**Composition of the Board:**

| | |
|---|---|
| **Chairman** | W. Sekretaruk |
| **Members:** | R. de Man |
| | M. Müller |

## Summary of Facts and Submissions

I. The applicant (appellant) appealed against the decision of the examining division refusing European patent application No. 06789683.7, filed as international publication PCT/US2006/031298 and published as WO 2007/021888.

II. The decision under appeal cited the following two documents, which are family members:

D1: WO 02/057906 A2, 25 July 2002; and
D2: US 2004/0059895 A1, 25 March 2004.

Alternately referring to both documents, the examining division decided that the subject-matter of claims 1 to 4, 6 to 9 and 11 to 17 of the then main request lacked inventive step within the meaning of Article 56 EPC and that the subject-matter of claims 5, 10 and 18 of the then main request and of claims 1 and 11 of the then first auxiliary request was insufficiently disclosed within the meaning of Article 83 EPC. Under the heading "OBITER", the decision contained further remarks on inventive step.

III. In the statement of grounds of appeal, the appellant maintained both its substantive requests. It requested reimbursement of the appeal fee because the examining division had committed a substantial procedural violation by failing to provide a reasoned decision in accordance with Rule 111(2) EPC for refusing the first auxiliary request.

IV. In a communication accompanying a summons to oral proceedings, the board introduced the following documents:

D3: US 5802339, 1 September 1998;

D4: US 6643762 B1, 4 November 2003; and

D5: "Register renaming", Wikipedia, 11 July 2005, retrieved from https://en.wikipedia.org/w/index.php?title=Register_renaming&oldid=18575902.

*Inter alia* it expressed the provisional opinion that the subject-matter of claim 1 of the main request lacked inventive step in view of document D1 and that the subject-matter of claim 1 of the first auxiliary request was sufficiently disclosed but lacked inventive step in view of document D3. The examining division's refusal of the first auxiliary request appeared to have been sufficiently reasoned.

V. With a letter dated 9 February 2017, the appellant filed a second auxiliary request. With a further letter dated 6 March 2017, the appellant filed a new second auxiliary request and a third auxiliary request and maintained its previous second auxiliary request as a fourth auxiliary request.

VI. In the course of oral proceedings held on 9 March 2017, the appellant submitted a new request labelled "replacement second auxiliary request" and maintained none of its other requests. At the end of the oral proceedings, the chairman announced the board's decision.

VII. The appellant requested that the decision under appeal be set aside and that a patent be granted with the following documents:

- claims 1 to 15 of 9 March 2017;

- description pages 2, 2a, 3, 4 and 6 of 9 March 2017;
- drawing, figure 1, of 9 March 2017;
- description pages 1, 5, 7 and 8 as published;
- drawing, figure 2, as published.

VIII. Independent claim 1 reads as follows:

"A system comprising a pipeline processor having a register file for storing operands required by the pipeline processor for the execution of instructions, the register file comprising:

a plurality of registers (200), each register comprising a plurality of memory cells, each register including a first one of the plurality of memory cells of the register to store a ready signal indicating whether data in the register is valid or invalid;

a decoder (202) configured to receive a first address of a target register selected from the plurality of registers and generate a control signal which selects the target register, in response to the received first address; and

logic (204) configured to gate the control signal with a ready signal stored in a first memory cell of the target register to disable a read operation to the target register when the stored signal in the first memory cell of the target cell is a ready signal indicating that the data in the register is invalid and enable a read operation to the target register when the signal stored in the first memory cell of the target register is a ready signal indicating that the data in the register is valid;

wherein data in the target register is invalid when a result of execution of an instruction to be written to the target register has not yet been stored in the target register."

Claims 2 to 9 are dependent on claim 1.

Independent claim 10 reads as follows:

"A method of accessing a register file in a pipeline processor, the register file for storing operands required by the pipeline processor for the execution of instructions, the register file having a plurality of registers (200), comprising:

receiving an address of a first register of a plurality of registers, the first register having a first memory cell to store a ready signal and a plurality of remaining memory cells to store data; and

storing a ready signal indicating that data in the register is valid in the first memory cell of the first register when data stored in the first register is valid and having the ready signal indicating that data in the register is not valid in the first memory cell of the first register when the data stored in the first register is invalid;

generating, within the register file, a control signal which selects the target register, in response to the received first address;

gating, within the register file, the control signal with the ready signal stored in the first memory cell of the target register to:

disable a read operation to the first register when a ready signal indicating that data in the register is invalid is stored in the first memory cell of the first register; and

enable the read operation to the first register when a ready signal indicating that data in the register is valid is stored in the first memory cell of the first register;

wherein data in the target register is invalid when a result of execution of an instruction to be written to the target register has not yet been stored in the target register."

Claims 11 to 15 are dependent on claim 10.

## Reasons for the Decision

1. The appeal complies with the provisions referred to in Rule 101 EPC and is therefore admissible.

2. *The invention*

2.1 The application relates to register files of pipeline processors. The background section explains that during execution of a series of instructions, the new value of a register is not always immediately written back to the register file corresponding to the register but often directly forwarded within the processor's pipeline for processing by a subsequent instruction. As a result, the register file may at times hold invalid data which must not be used for instruction execution. Power expended on read operations on such data is therefore wasted.

2.2 The invention essentially proposes including in each register of the register file a memory cell for storing a "ready signal" indicating whether the data held in the register is valid or invalid. Upon receipt of a target register address in the context of a read operation, decoder logic of the register file generates a control signal selecting the target register. This control signal is gated with the ready signal either to disable the read operation if the ready signal

indicates that the register holds invalid data, or otherwise to enable the read operation.

3. *Added subject-matter – Article 123(2) EPC*

Independent system claim 1 and corresponding independent method claim 10 find a basis in claims 1 to 4 and paragraphs [0012] to [0015] and [0017] of the application as originally filed. The board has no reason to question the basis for the dependent claims.

The application thus complies with Article 123(2) EPC.

4. *Sufficiency of disclosure – Article 83 EPC 1973*

4.1 Claim 5 of the main request considered in the decision under appeal included a feature to the effect that a register's ready signal was set to invalid when an instruction writing to that register was detected in the pipeline. The examining division decided that the application did not sufficiently disclose the subject-matter of that claim, essentially because it did not explain how to deal with a read instruction shortly preceding the write instruction, which might need to read the (old) value held in the register at a time when the write instruction had already been detected and, consequently, the register's ready signal had already been set to invalid.

4.2 Present independent claims 1 and 10 relate to a pipeline processor and do not define measures preventing the scenario described by the examining division, nor are such measures discussed in the application. In addition, present dependent claim 4 corresponds to dependent claim 5 objected to by the examining division. The board, however, does not share

the examining division's view. Admittedly, the design of a correctly functioning processor pipeline does involve many intricate details, and the application scarcely deals with any of them. But since such designs were known at the priority date of the application, the board sees no reason to doubt that the skilled person, who is familiar with the basic techniques in his field, was able to carry out the invention on the basis of his common general knowledge. In particular, register renaming was a customary technique to resolve the so-called false "write-after-read" dependencies hinted at by the examining division; see in this context document D5.

4.3 Hence, the board considers that the application complies with Article 83 EPC 1973.

5. *Inventive step – Article 56 EPC 1973*

5.1 *Documents D1 and D2*

5.1.1 Document D1 (which is essentially identical in content to document D2) discloses on page 9, lines 15 to 19, a microprocessor circuit including a register file and an auxiliary register. The register file has eight registers, and each register is assigned a bit of the auxiliary register indicating, as document D1 puts it on page 9, lines 31 to 37, whether or not data is stored in the register.

In the embodiments described in document D1, a value "1" in a bit of the auxiliary register indicates that the register corresponding to that bit holds valid data, and a value "0" indicates that no data has yet been written to it (page 10, lines 20 to 23; page 10, line 36, to page 11, line 6).

5.1.2 According to the description on page 11, line 33, to page 12, line 8, when data is written to a register of the register file, the corresponding bit of the auxiliary register is set to "1". To read data from a register, first the corresponding bit of the auxiliary register is checked. If that bit is set to "0", then the value 0 is returned independently of the content of the register. Only if the bit is set to "1" is the data held in the register actually read out.

5.1.3 Thus the auxiliary register of D1 allows the processor to clear one or more registers in an (energy-)efficient manner by simply writing a "0" to each of the corresponding bits of the auxiliary register. Once this is done, a cleared register will return the value 0 until a value is written to it (which will automatically set the bit in the auxiliary register to "1").

5.1.4 Although the processor of document D1 bears similarity to the processor of the present invention in that each register of the processor's register file is provided with a "validity bit" indicating whether or not the register holds valid data and preventing the reading out of invalid data, the broader purpose of the validity bits of document D1 is quite different. In the present invention, the validity ("ready signal") bits are part of the processor's pipeline design; the feature of claim 1 specifying that "data in the target register is invalid when a result of execution of an instruction to be written to the target register has not yet been stored in the target register" excludes other interpretations. In document D1, the validity bits are used in the execution of specific instructions for clearing one or more registers. This is useful, for

example, in smart cards where untrusted code is not allowed to read the values stored in registers by security-sensitive code (see page 2, lines 11 to 35, and page 4, lines 13 to 16). Document D1 in fact does not mention whether the microprocessor includes a pipeline.

5.1.5 The skilled person starting from document D1 may well decide to include a processor pipeline, but in the course of routine development he would not normally go against the technical teaching of document D1 and modify its circuit to use the bits of the auxiliary register for the different purpose of keeping track of which registers temporarily hold values that are invalid due to write instructions still pending in the processor's pipeline. So starting from document D1 the skilled person would not arrive in an obvious manner at the subject-matter of claim 1.

5.1.6 Under the heading "OBITER", the examining division essentially argued that the problem of providing not stale data but valid source operands to instructions was well-known in the art and that paragraph [0025] of document D2 (which corresponds to the paragraph bridging pages 5 and 6 of document D1) disclosed setting the ready signal of a register to invalid in order to ensure that its invalid content was not read. The skilled person would consider it a normal design procedure to use the same technique to prevent reading of invalid data during instruction execution and ensure data correctness.

Documents D1 and D2 are, however, not concerned with processor pipelines and avoiding the use of stale data. Thus, although processor pipelines and the need to avoid using stale register data were indeed known to

the skilled person (see document D4, column 1, lines 19 to 36, and document D5, "Hazards and Renaming" section), he would not consider documents D1 and D2 when looking for a technique to detect that the data held in a register is stale.

5.1.7 Hence, the subject-matter of claim 1 is not rendered obvious by document D1 or the corresponding document D2.

5.2 *Documents D3 and D4*

5.2.1 Document D3 discloses a high-performance X86 processor comprising multiple functional units capable of performing parallel speculative execution, including "Numerics Processor", "Integer Execution" and "Address Preparation" units (column 1, lines 12 to 24). It also comprises a decoder unit, which fetches and decodes instructions and generates pseudo-operations (p-ops) that are broadcast to functional execution units (column 1, lines 25 to 32, 66 and 67).

As explained in column 1, line 66, to column 2, line 12, the execution units queue incoming p-ops and are free to execute their p-ops largely independently of the other execution units. Hence instructions are processed in multiple overlapping stages, which means that the processor includes a pipeline. (See also column 6, lines 56 to 64, "Pipeline performance".)

Document D3 discloses in column 2, lines 47 to 63, that dependencies may exist between instructions that force one execution unit to wait for the register value computed by another unit to become available.

5.2.2 Document D3 proposes adding a supplemental "Add/Move Unit (AMU)" execution unit to the existing execution units of the high-performance processor (column 3, lines 28 to 32). According to column 5, line 59, to column 6, line 9, the AMU shares with the "Address Preparation unit" (AP) the use of two read ports and one write port to the AP's register file. This register file includes a set of validity ("register valid") bits, which indicate whether a register holds a "valid" result. When the decoding unit issues a p-op, the AP clears the validity bit associated with the destination physical register specified by the p-op. This validity bit "is used as an interlock for both effective address generation in AP 500 and computation by the AMU 100". It becomes set again whenever a result is written into the destination physical register.

5.2.3 Thus, document D3 discloses a register file comprising a plurality of registers and a set of validity bits, each validity bit indicating whether the value stored in an associated register is valid. When a "write instruction", i.e. an instruction writing to a target register, is detected in the pipeline, the register valid bit associated with the target register is cleared to indicate that the register holds an invalid result. When a "read instruction", i.e. an instruction reading from a source register, is encountered, the register valid bit associated with the source register is checked, and execution of the read instruction is stalled until the register's value becomes valid.

5.2.4 Document D3 does not disclose that the memory cell storing the validity bit for a particular register is one of the memory cells forming that register. And more significantly, although both the register file and the set of validity bits are located in the AP (as shown in

Figure 1), there is no indication in document D3 that – as in the claimed invention – a single read operation performed on the register file results in a signal selecting the target register and being gated with the validity bit. Were the skilled person to fill in the implementation details missing in document D3, he would probably let the processor first read out the validity bit in a first read operation and then – if or when the validity bit indicates that the target register holds valid data – read out the target register in a second read operation. In any event, document D3 neither discloses nor suggests the particular register file implementation which is now claimed and which allows read operations to be executed efficiently.

5.2.5 The subject-matter of claim 1 is therefore not rendered obvious by document D3 alone. And starting from document D3, the skilled person would have no incentive to consider the register file of document D1, which addresses the problem of efficiently clearing registers rather than that of efficiently reading them out.

5.2.6 Like document D3, document D4 discloses a pipeline processor comprising a register file containing registers read from and written to by instructions (column 1, lines 19 to 26; column 2, lines 23 to 26). Each register is associated with a validity bit in a "scoreboard" register file indicating whether data produced by an earlier executed instruction has yet to be written to the register (column 2, lines 12 to 23). Document D4 is not closer to the claimed invention than document D3.

5.3 In sum, the subject-matter of independent claim 1 is not rendered obvious by the available prior art and thus involves an inventive step within the meaning of

Article 56 EPC 1973. The same is true for the subject-matter of corresponding independent claim 10.

6. Since, moreover, the description has been adapted, the application complies with the requirements of the EPC. The appeal is therefore to be allowed.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a European patent with the following documents:

- claims 1 to 15 of 9 March 2017;
- description pages 2, 2a, 3, 4 and 6 of 9 March 2017;
- drawing, figure 1, of 9 March 2017;
- description pages 1, 5, 7 and 8 as published;
- drawing, figure 2, as published.

The Registrar: The Chairman:

B. Atienza Vivancos W. Sekretaruk

Decision electronically authenticated