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**Datasheet for the decision
of 11 May 2017**

Case Number: T 1202/12 - 3.4.03

Application Number: 06017548.6

Publication Number: 1761120

IPC: H05K3/28

Language of the proceedings: EN

Title of invention:
Wired circuit board

Applicant:
NITTO DENKO CORPORATION

Headword:

Relevant legal provisions:
EPC 1973 Art. 56

Keyword:
Oral proceedings - withdrawal of request for oral proceedings
Inventive step - (no)

Decisions cited:
T 0482/92

Catchword:



Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 1202/12 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 11 May 2017

Appellant: NITTO DENKO CORPORATION
(Applicant) 1-2, Shimo-hozumi 1-chome
Ibaraki-shi,
Osaka 567-8680 (JP)

Representative: Schwabe - Sandmair - Marx
Patentanwälte Rechtsanwalt
Partnerschaft mbB
Joseph-Wild-Straße 20
81829 München (DE)

Decision under appeal: Decision of the Examining Division of the
European Patent Office posted on 13 December
2011 refusing European patent application No.
06017548.6 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman G. Eliasson
Members: M. Papastefanou
C. Heath

Summary of Facts and Submissions

- I. The appeal is against the decision of the examining division refusing European patent application No. 06 017 548.6 on the ground that the claimed subject matter did not involve an inventive step within the meaning of Article 56 EPC.
- II. The appellant requested that the decision of the examining division be set aside and that a patent be granted on the basis of the request filed with the grounds of appeal. As an auxiliary measure, the holding of oral proceedings was requested in case the board would not be minded to accept this request.
- III. The following documents, cited in the appealed decision, are considered to be relevant:
- D2: WO 2005/055683 & EP 1 581 032 A
D4: US 6 900 967 B1
D6: US 2004/221447 A1.
- IV. In a communication pursuant to Article 15(1) of the Rules of Procedure of the Boards of Appeal (RPBA), which was annexed to summons to oral proceedings, the board communicated its preliminary, non binding opinion to the appellant.

The board made additional reference to the documents:

- D8: JP 10 12983 (discussed in paragraphs [0004]-[0006] of the present application); and
D8a: Automatic English translation of D8 provided by the website of the Japanese patent office.

According to the board's preliminary opinion, the subject matter of claim 1 of the sole request did not involve an inventive step in the sense of Article 56 EPC in view of the obvious combination of documents D2 with D8/D8a. According to its auxiliary request, the applicant was therefore summoned to oral proceedings.

- V. After receiving this communication and the summons to oral proceedings, the appellant withdrew its request for oral proceedings and requested a decision "on the state of the file".
- VI. Following the appellant's reaction, the board cancelled the oral proceedings and issues its decision in writing.
- VII. Claim 1 of the sole request has the following wording:

*A wired circuit board (1) comprising:
an insulating base layer (3);
a seed film (11) formed on the insulating base layer (3);
a conductive pattern (4) formed on an upper surface of the seed film (11);
a metal oxide layer (5) formed to continuously cover an upper surface and a side surface of the conductive pattern(4); and
an insulating cover layer (6) formed over the insulating base layer (3) to cover the conductive pattern (4) covered by the metal oxide layer (5);
characterized in that:
the seed film (11) is formed only in a part corresponding to the conductive pattern (4) and the metal oxide layer (5) is formed to continuously extend to interpose between the conductive pattern (4) and the*

insulating cover layer (6) and between the insulating base layer (3) and the insulating cover layer (6), a lower end portion of the metal oxide layer (5) covering the side surface of the conductive pattern (4) being in contact with a side end surface of the seed film (11), the thickness of the metal oxide layer (5) being 5 to 300 nm; and a surface resistance of the metal oxide layer (5) being not less than $10^{12} \Omega / \square$; wherein the oxide layer (5) functions as a barrier layer to the conductive pattern (4) to prevent the metal from forming the conductive pattern (4) from diffusing in the insulating cover layer.

Reasons for the Decision

1. With the withdrawal of its request for oral proceedings, the appellant requested a decision "on the state of the file". The board interprets this as a request for a decision based on the written procedure so far.
2. Closest prior art
 - 2.1 According to the established case law of the Boards of Appeal, the closest prior art for assessing inventive step is normally a prior art document disclosing subject-matter conceived for the same purpose as the claimed invention and having the most relevant technical features in common (T 482/92, Reasons, point 4.1, third paragraph).
 - 2.2 In the appealed decision, the examining division considered document D4 to represent the closest prior art. In view of the amendments of the claims in appeal,

the board considers document D2 to be the most appropriate starting point for the skilled person.

- 2.3 Document D2 discloses (using the terminology of claim 1) a wired circuit board comprising an insulating base layer (*substrate 1*, Figure 2, Figure 4) upon which a conductive pattern (2, Figure 2, Figure 4) is formed. The conductive pattern is covered by a metal oxide layer (3, paragraph [0044]) formed to continuously cover an upper surface and a side surface of the conductive pattern (Figure 4, paragraph [0045]), and an insulating cover layer (6, Figure 7E, paragraph [0051]) formed over the insulating base layer to cover the conductive pattern covered by the metal oxide layer. The metal oxide layer is formed to continuously extend to interpose between the conductive pattern and the insulating cover layer (Figure 7E) and to act as a barrier layer to the conductive pattern to prevent the metal of the conductive pattern from diffusing in the insulating cover layer (paragraph [0037]).
- 2.4 The circuit board of D2 does not comprise a seed film formed between the insulating layer and the conductive pattern, which is formed only in a part corresponding to the conductive pattern. In addition, as shown in Figure 7D and 7E, the metal oxide film does not extend to cover the entire surface of the substrate 1 - i. e. does not interpose between the insulating base layer and the insulating cover layer. The thickness of the metal oxide layer in D2 is 500 - 5000 nm (paragraph [0042]) and there is no mention of any value for its surface resistance.
- 2.5 Regarding the coverage of the surface of the substrate by the metal oxide layer, it is stated in D2 (paragraph [0053]) that it is not necessary to cover the whole

area of the substrate with the metal oxide layer as it is sufficient to cover the conductive pattern in order to insulate and protect it. However, with reference to Figure 6, it is specifically stated in the same paragraph that coverage of the whole surface of the substrate by the metal oxide layer would increase the reliability of the insulation in cases where a more dense conductive pattern is needed on the substrate.

3. Differences and technical problem

3.1 Hence, the wired circuit board of claim 1 differs from that described in Figure 7D and 7E of D2 in that a seed film is formed between the insulating base layer and the conductive pattern and that the metal oxide layer covers the whole surface of the insulating base layer (substrate). The wired circuit of D2 has no such seed film and the metal oxide layer covers only the conductive pattern. Furthermore, the metal oxide layer in claim 1 has a thickness of 5-300nm and a surface resistance of no less than $10^{12} \Omega/\square$.

3.2 In the application, an additive patterning process is used for forming the conductive pattern, which allows a higher density wiring (paragraph [0033]). The formation of the seed film (ground layer), upon which the conductive pattern is formed, is part of this additive process (paragraph [0032]). Hence, the use of a seed film would indicate high - density wiring for the circuit board. According to D2, the same purpose is achieved by covering the whole surface of the substrate (insulating base layer in the terminology of claim 1) by the metal oxide layer (see also paragraph 3.2 above). Hence, starting from D2 the technical problem to be solved is to provide a circuit board with increased wiring density.

4. Document D8

4.1 Document D8 (the passages cited below refer to D8a unless otherwise indicated) relates to the manufacture of a substrate for wired circuit board of high density ("*high capacity*" - paragraph [0047]). As described in Figure 1 and 2, the circuit board comprises an insulating base layer (7) upon which a seed film (*thin chrome film* 23) is formed. On the seed film, a conductive pattern (*layer* 3) is formed. This conductive pattern is protected by a thin film (28). Finally, the whole surface of the circuit board is covered by a coating layer (8). As it can be seen in Figure 10, the seed film is patterned corresponding to the conductive pattern (see also paragraph [0058]).

5. Obviousness

5.1 The skilled person starting with the circuit board described in Figures 7D and 7E of D2 and wishing to provide a circuit board of increased wiring density, would select a suitable and known patterning process that allows for higher density wiring for its manufacture. As described above, such a process would be an additive process such as that described in D8, which foresees the forming of a seed film between the insulating base layer and the conductive pattern. In addition, as already hinted in D2 itself, to allow for high wiring density, the coverage of the metal oxide layer would have to be extended to cover the whole surface of the insulating base layer, as in Figure 6 of D2. With such a construction, a lower end portion of the metal oxide layer covering the surface of the conductive pattern would also be in contact with a side

end surface of the seed film, as it is shown in Figure 6 of D2 and Figure 2 and 3 of D8.

- 5.2 Regarding specific values for the thickness of the metal oxide layer, the board notes that in D2 there is mention of a metal oxide layer thickness between 500 - 5000 nm (paragraphs [0023] and [0042]). These values would refer to the main embodiment as presented in Figure 7D and 7E. In a circuit board of higher wiring density, it would be expected that the metal oxide layer would have a smaller thickness than that. In D8, where the wiring density of the circuit board is higher than in the board of D2, there is mention of a thickness between 50 - 100 nm for the covering (barrier) layer (paragraph [0059]). The skilled person would, thus, adapt the thickness of the metal oxide layer in D2 in order to allow for higher wiring density. The thickness value range of 50 - 100 nm suggested in D8 falls within the claimed range.
- 5.3 Regarding the surface resistance, since the metal oxide layer is supposed to be used as a barrier layer, the skilled person would know that relatively high values for the surface resistance are called for. In D6, for example, where a method of producing wired circuit boards similar to the one of D2 is described (Figure 1 and paragraphs [0033] - [0043]), a metal oxide layer of very large surface resistance is used as a barrier (paragraphs [0041], [0059], [0063]). The range of values for the surface resistance of this layer is 10^{10} - 10^{13} Ω/\square (paragraphs [0092], [0093]). It is considered, hence, that the specific value of 10^{12} Ω/\square that is defined in claim 1 would be within the expected range and, hence, an obvious selection for the skilled person.

5.4 The appellant has not provided any comments or counter-arguments to the above objections.

6. For the above reasons, the subject matter of claim 1 does not involve any inventive step in the sense of Article 56 EPC 1973.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:



S. Sánchez Chiquero

G. Eliasson

Decision electronically authenticated