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## Datasheet for the decision
## of 8 January 2018

**Case Number:** T 1157/12 - 3.5.06

**Application Number:** 01991757.4

**Publication Number:** 1346282

**IPC:** G06F9/38, G06F9/30

**Language of the proceedings:** EN

**Title of invention:**
SIGNAL PROCESSING DEVICE AND METHOD FOR SUPPLYING A SIGNAL
PROCESSING RESULT TO A PLURALITY OF REGISTERS

**Applicant:**
Intel Corporation

**Headword:**
Supplying a result to a plurality of registers/INTEL

**Relevant legal provisions:**
EPC 1973 Art. 56, 84, 83
EPC Art. 123(2)

**Keyword:**
Inventive step - (yes)
Claims - clarity (yes)
Sufficiency of disclosure - (yes)
Amendments - added subject-matter (no)

EPA Form 3030
This datasheet is not part of the Decision.
It can be changed at any time and without notice.

**Decisions cited:**

**Catchword:**

Beschwerdekammern

Boards of Appeal

Chambres de recours

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**Case Number: T 1157/12 - 3.5.06**

D E C I S I O N
of  Technical Board of Appeal 3.5.06
of 8 January 2018

| | |
|---|---|
| **Appellant:**<br>(Applicant) | Intel Corporation<br>2200 Mission College Boulevard<br>Santa Clara, CA 95054 (US) |
| **Representative:** | V.O.<br>P.O. Box 87930<br>2508 DH Den Haag (NL) |
| **Decision under appeal:** | **Decision of the Examining Division of the European Patent Office posted on 10 November 2011 refusing European patent application No. 01991757.4 pursuant to Article 97(2) EPC.** |

Composition of the Board:

| | |
|---|---|
| **Chairman** | W. Sekretaruk |
| **Members:** | A. Teale |
| | G. Zucka |

## Summary of Facts and Submissions

I.      This is an appeal against the decision, dispatched with
        reasons on 10 November 2011, refusing European patent
        application No. 01 991 757.4 on the basis that the
        claims according to a main and an auxiliary request
        contained added subject-matter, Article 123(2) EPC, and
        were unclear, Article 84 EPC. In addition, the
        invention was found to be insufficiently disclosed,
        Article 83 EPC.

II.     A notice of appeal and the appeal fee were received on
        4 January 2012.

III.    With a statement of grounds of appeal, received on
        12 March 2012, the appellant submitted amended claims
        and description pages according to a new main and a new
        auxiliary request. The appellant requested that a
        patent be granted on the basis of said main or
        auxiliary request and made an auxiliary request for
        oral proceedings.

IV.     The application is thus being considered in the
        following form:

        **Description**
        Main request: page 1 as originally filed and pages 2,
        2a and 3 to 6 (main request), received with the grounds
        of appeal.
        Auxiliary request: page 1 as originally filed and pages
        2, 2a and 3 to 6 (auxiliary request), received with the
        grounds of appeal.

        **Claims (all received with the grounds of appeal)**
        Main request: 1 to 11.
        Auxiliary request: 1 to 10.

**Drawings (both requests):**

Pages 1/4 to 4/4, as originally filed.

V.      The independent claims according to the main request
        read as follows:

"1. A signal processing device comprising a plurality
of functional units (UCl-UCn) for processing digital
data based on an instruction word, and a plurality of
register files (RFl-RFn) for storing results obtained
from respective ones of said functional units, wherein
said functional units are arranged to supply a result
and a logical register address derived from respective
instructions in said instruction word, characterized by
register allocation means (RA), wherein the functional
units are arranged to supply the result and the logical
register address to the register allocation means (RA),
and wherein the register allocation means (RA) are
arranged for selecting at least two of said register
files (RFl-RFn) and for supplying said result and said
logical register address or a register address derived
from the logical register address to said selected
register files, if said instruction word comprises a
corresponding indication."

"8. A method of supplying a signal processing result to
a plurality of registers arranged in different register
files (RAl-RAn) of a signal processing device, said
method comprising the steps of:
a) determining a logical register address based on an
instruction in an instruction word, and
b) supplying said logical register address or an
address derived from the logical register address to
said plurality of register files, characterized by the
steps of

c) selecting said different register files based on a
corresponding indication in said instruction word and
supplying said logical register address or said derived
address to said selected register files."

VI.      The wording of the claims according to the auxiliary
         request is not material to this decision.

**Reasons for the Decision**

1.       Admissibility of the appeal

         In view of the facts set out at points I to III above,
         the appeal fulfills the admissibility requirements
         under the EPC and is consequently admissible.

2.       Summary of the invention

2.1      The application relates to a digital signal processor
         (DSP) using VLIW ("Very Large Instruction Words")
         containing a plurality of instructions so that a
         plurality of partial tasks are processed in parallel by
         individual functional units, i.e. pipeline stages.

2.2      The DSP uses "data stationary" instruction encoding,
         understood by the board to mean that an instruction
         travels together with associated data in a pipeline and
         controls the sequence of operations performed on these
         data in each pipeline stage. A consequence is that
         complex hardware is required to buffer data path
         control information supplied by the processor
         sequencer. The results from the functional units are
         stored in register files comprising a plurality of
         register files (RF) addressable using a "result
         register index" (RRI). Often a functional unit can only

read its operands from, or write its result to, a
subset of register files. If a register file is
inaccessible to a functional unit, then a copy of the
variable has to be written to an accessible register
file. The writing of a result in the same cycle to
multiple register files is termed "broadcasting" or
"multicasting".

2.3      In a data stationary processor an output port of the
         functional unit has to select one of multiple result
         buses to which the register file write ports are
         connected to perform a write operation. This leads to
         an undesirable increase in processor cost when
         implementing a broadcasting function, the board
         understanding that the extra cost is caused by extra
         complexity. The invention is thus directed to the
         problem of reducing device complexity in implementing a
         broadcasting function; see page 2a, lines 9 to 10. The
         invention solves this problem by overlapping register
         address spaces; see page 3, lines 10 to 11. This is
         achieved by addressing several register files using the
         same logical register address; see page 3, lines 4 to
         6. This has the effect that copy operations between
         register files can be eliminated, since, as shown in
         figures 1 and 4, the result data and a logical register
         address are supplied to a register file allocation
         means (RA) which generates result register indices
         (RRI) to select at least two register files (RF1-RFn)
         and supplies the result data and the RRI to the
         selected register files. Hence the results of the
         functional units (see "Result data") are broadcast to
         multiple registers of different register files in a
         single processor cycle; see figure 1, page 3, lines 7
         to 10, and page 4, lines 9 to 19.

2.4     Figure 2 shows how the result values (D1-Dn) and
        logical register addresses (RI) produced by the
        functional unit clusters (UC) are passed to the
        register file allocation unit (RA); see page 4, line
        20, to page 5, line 7. As a result, any of the result
        data (D1-Dn) and logical register addresses (RI) can be
        distributed to any or several partitioned register
        files (RF1-RFn) to realize a broadcasting or
        multicasting function. Figure 4 shows corresponding
        steps of a broadcasting method.

2.5     According to page 4, lines 16 to 19, the register file
        allocation unit (RA) may be implemented using a
        demultiplexer, as shown in figure 3, which shows a
        register file allocation unit (RA) implemented by three
        de-multiplexers (DM1-DM3) feeding two OR-gates; see
        page 5, lines 20 to 29.

3.      Added subject-matter, Article 123(2) EPC

3.1     According to the original description, for instance
        page 3, lines 18 to 21, the instruction word may either
        comprise a corresponding control or flag information
        indicating the broadcasting or multicasting function or
        may include a specific result register address
        indicating multicast or broadcast registers in the
        selected register files. The board understands the
        second option to mean that the result index is part of
        the instruction word.

3.2     A recurring question in the appealed decision is
        whether, as the decision concludes, the original
        application only disclosed the instruction word
        containing a single register index (RI) or whether, as
        the appellant has argued, the original application
        disclosed each instruction in the instruction word

comprising a register index (RI). In the light of
figure 3, which shows a register index RI associated
with each of two functional unit clusters (UC1, UC2),
and its description (see page 5, lines 20 to 29), the
board agrees with the appellant. Each functional unit
cluster in figure 3 receives variables (which the board
understands as "operands"; two in the case of UC1 and
three in the case of UC2) and a register index RI from
the instruction word. In the board's opinion, it does
not make technical sense in the context of the
application that there only be one register index in
the instruction word, since the VLIW DSP is designed to
execute several independent instructions contained in
each instruction word in parallel; see page 1, lines 21
to 22. In the board's view the independence of the
instructions requires that each instruction have its
own register index.

3.3      Hence the concept set out in claim 1 of both requests
         in the decision and in claim 1 of the present main
         request that "said functional units are arranged to
         supply a result and a logical register address derived
         from respective instructions in the instruction word"
         is properly based on the disclosure in the original
         application, thus overcoming this reason for the
         decision. Claim 8 is also properly based on the
         original disclosure for the same reasons.

3.4      According to the decision, the original description
         stated that the result register index (RRI) was derived
         from the result index (RI) output by the functional
         unit and not from the instruction in the instruction
         word or from the instruction word itself. Claim 1 of
         both then requests had been amended to contain the
         expression "the result register index (RRI) derived

from the respective instruction comprised in said
instruction word", a concept not originally disclosed.

3.5     Claim 1 of the present main request has been amended to
        state that the logical register address, understood as
        the RRI, produced by the register allocation means (RA)
        is based on the result from the functional units and
        the logical register address derived from instructions
        in the instruction word. In the board's view, the
        present expression is consequently properly based on
        the original disclosure, thus overcoming this reason
        for the decision.

3.6     The board is satisfied that the amendments to claim 1
        of the main request, and to corresponding method claim
        8, satisfy Article 123(2) EPC regarding added subject-
        matter.

4.      Clarity, Article 84 EPC 1973

4.1     According to the decision, claim 1 of both requests was
        unclear due to the use of the expression, relating to
        the selection of one or more register files, "an
        information in said instruction word" and because of
        the reference, in relation to writing the result data
        (D1-Dn) to the "addressed register" of the selected
        register files. It was unclear what the "information"
        in said instruction word was or how it related to the
        "result index (RI1-RIn)" in the instruction, mentioned
        elsewhere in the claim.

4.2     Claim 1 of the main request now uses the different
        expression "wherein said functional units are arranged
        to supply a result and a logical register address
        derived from respective instructions in said
        instruction word" and does not refer to "an

information" or a "result index". Hence claim 1
overcomes this reason for the appealed decision.

4.3     According to the decision, it was unclear how the
        result register index (RRI) in claim 1 of both requests
        was derived from the instruction in the instruction
        word. In the board's view, the description discloses a
        register index (RI) in the instruction word firstly
        being passed unchanged through the register allocation
        means (RA) and secondly being modified by the register
        allocation means (RA) (see page 4, lines 10 to 14). The
        board takes the view that the "logical register
        address" produced by the functional unit and converted
        by the register allocation means (RA) into a result
        register index (RRI), set out in claim 1 of the present
        main request, is broad, in the sense that it is not
        limited to a particular derivation method, but is not
        unclear. Moreover the example given in figure 3 shows
        how the result register indices (RRI) can be generated.
        Hence claim 1 also overcomes this reason for the
        decision.

4.4     The board is satisfied that claim 1 and corresponding
        method claim 8 of the present main request are clear,
        Article 84 EPC 1973.

5.      Sufficiency of disclosure, Article 83 EPC 1973

5.1     According to point 14.1 of the reasons for the
        decision, the application insufficiently discloses how
        the register indices (RI1-RIn) are derived from a
        single result index RI in the instruction word.

5.2     As stated above, the board takes the view that the
        application discloses each instruction in the
        instruction word having its own register index.

Moreover, in the light of figure 3 and page 5, lines 13 to 19, the result index RI specified for a variable in the instruction word may correspond, in the global register address map, to a broadcast/multicast register in different register files having the result register index RRI. In other words, the register index RI is mapped to particular result register indices RRI. This understanding of the invention is consistent with the statement on page 3, lines 10 to 11, that broadcasting is implemented by overlapping register address spaces, a concept which the skilled person would have understood and been able to implement without undue burden. The embodiment in figure 3 gives a concrete example of how this may be implemented, since the register index RI in the instruction word controls each of the three de-multiplexers DM1-DM3 so that the results from functional unit clusters UC1 and UC2 can be selectively supplied (thus mapping RI to a choice of RIIs), via the two OR-Gates to the inputs of register files RF1 and RF2; see the register indices RRI indicated at their inputs.

5.3     Hence the board is satisfied that the application discloses the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art, Article 83 EPC 1973.

6.      Document D1

6.1     As illustrated in figure 6, D1 concerns a pipelined VLIW processor (see page 2, lines 4 to 5) having a plurality of functional units (620,622,624,626), each being associated with a segment (610,612,614,616) of a multiported register file (602). According to the paragraph bridging pages 7 and 8, an instruction word always includes one instruction for execution in the

general functional unit (GFU) and up to three
instructions for execution in the media functional
units (MFU). A MFU instruction field within the VLIW
instruction word can include an opcode (understood by
the board as an "operator"), three source register
fields and one destination register field. The board
understands each such field to contain register address
information. Each register file segment is partitioned
into global registers, which are read from, and written
to, by all functional units, and local registers, which
are read from, and written to, only by the associated
functional unit.

6.2     According to the abstract, "The local registers in a
        register file segment are addressed using register
        addresses in a local register range outside the global
        register range that are assigned within a single
        register file segment/functional unit pair. Register
        addresses in the local register range are the same for
        the plurality of register file segment/functional unit
        pairs and address registers locally within a register
        file segment/functional unit pair."

        The global registers can be addressed by all
        functional units as 0-95, but each functional unit
        uses a different address range to address its own
        local registers, such as 96-127, 128-159, 160-191 and
        192-223, respectively, for the four functional units;
        see page 13, lines 4 to 15.

        As figure 6 shows, the result from each functional unit
        is passed to its global registers, meaning that the
        result is available as an input to not only that
        particular functional unit but to all the others as
        well.

7.        Inventive step, Article 56 EPC 1973

7.1       In a communication dated 27 December 2007 the examining
          division raised an inventive step objection against a
          previous version of claims 1 and 8 on the basis that
          their subject-matter only differed from the disclosure
          of D1 in setting out a plurality of register files,
          while D1 disclosed a plurality of register file
          segments located in one register file. The objective
          technical problem was seen as finding an alternative to
          the known processing device, and the storage of the
          results from the functional units in a respective
          register file (as claimed) or a respective register
          file segment (as known from D1) were both regarded as
          obvious alternatives not involving an inventive step.

7.2       Point 15.3 of the appealed decision states that, in
          contrast to the disclosure of D1, the register files in
          the application were arranged such that the logical
          register address range of a part of the file overlapped
          with that of other files, but not necessarily with all
          other files, as was the case in D1. The application was
          thus aimed at a cheaper (the board understands this to
          mean "simpler") form of broadcasting using a few
          physical registers with the same logical register
          address in different register files.

7.3       The appellant has stated that the subject-matter of
          claim 1 differs from the disclosure of D1 in that D1
          does not disclose the register file allocation unit
          (RA). In D1 data was exchanged by using global
          registers, and writing a result to a global register
          for one register file segment automatically overwrote
          the corresponding global register for all the other
          functional units. The objective technical problem was
          thus to allow the global registers of one register file

segment to be overwritten without overwriting the
global registers of all the other register file
segments. This was achieved by the register file
allocation unit (RA) allowing a register to be used as
a broadcast register or a unicast register.

7.4     The board agrees with the appellant that the subject-
        matter of claim 1 differs from the disclosure of D1 in
        that D1 does not disclose the register file allocation
        unit (RA). In the board's view, the objective technical
        problem formulated by the appellant, namely to allow
        the global registers of one register file segment to be
        overwritten without overwriting the global registers of
        all the other register file segments, is a fair one,
        and it is indeed solved by the characterising features
        setting out the register allocation unit.

7.5     Since D1 does not disclose, or even hint at, the
        characterising features, which are not themselves usual
        matters of design, the board finds that the subject-
        matter of claim 1 involves an inventive step, Article
        56 EPC 1973. As the method steps set out in claim 8
        correspond to the features of the device of claim 1,
        the subject-matter of claim 8 also involves an
        inventive step for the same reasons.

**Order**

**For these reasons it is decided that:**

The decision under appeal is set aside.
The case is remitted to the first instance with the order to
grant a patent in the following version:

Description: page 1 as originally filed and pages 2, 2a and 3
to 6 (main request), received with the grounds of appeal.

Claims: 1 to 11 (main request), received with the grounds of
appeal.

Drawings: pages 1/4 to 4/4, as originally filed.


The Registrar:                          The Chairman:


B. Atienza Vivancos                     W. Sekretaruk


Decision electronically authenticated