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Datasheet for the decision of 22 June 2017

Case Number: T 0945/12 - 3.5.07

Application Number: 07758147.8

Publication Number: 1997111

IPC: G11C7/10

Language of the proceedings: EN

Title of invention:
Memory device with mode-selectable prefetch and clock-to-core timing

Patent Proprietor:
Rambus Inc.

Former Opponent:
SK hynix Deutschland GmbH

Headword:
Memory device with prefetch modes/RAMBUS

Relevant legal provisions:
EPC Art. 54, 123(2)

Keyword:
Novelty - main request (no)
Amendments - intermediate generalisation - added subject-matter - auxiliary requests (yes)

Decisions cited:
G 0007/93, T 0133/92, T 2219/10, T 0971/11

Catchword:

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Case Number: T 0945/12 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 22 June 2017

Appellant: (Patent Proprietor)	Rambus Inc. 1050 Enterprise Way, Suite 700 Sunnyvale, CA 94089 (US)
Representative:	Eisenführ Speiser Patentanwälte Rechtsanwälte PartGmbB Johannes-Brahms-Platz 1 20355 Hamburg (DE)
Former Respondent: (Former Opponent)	SK hynix Deutschland GmbH Am Prime Parc 13 65479 Raunheim (DE)
Representative:	Ter Meer Steinmeister & Partner Patentanwälte mbB Nymphenburger Straße 4 80335 München (DE)
Decision under appeal:	**Decision of the Opposition Division of the European Patent Office posted on 22 February 2012 revoking European patent No. 1997111 pursuant to Article 101(3)(b) EPC.**

Composition of the Board:

Chairman	R. Moufang
Members:	P. San-Bento Furtado
	R. de Man

Summary of Facts and Submissions

I. The patent proprietor (appellant) appealed against the decision of the Opposition Division revoking European patent No. 1 997 111. The corresponding European application 07758147.8 was filed as international application PCT/US2007/063567 and published as WO 2007/106710.

II. The opposition against the patent had been filed by Hynix Semiconductor Deutschland GmbH on the grounds of lack of novelty, lack of inventive step and added subject-matter (Article 100(a) and (c) EPC). The following prior art documents were cited among others:

OD1: US 2005/0152210 A1, published on 14 July 2005;

OD2: US 6 185 149 Bl, published on 6 February 2001;

OD3: JP 10-172283 A, certified translation of the document published on 26 June 1998;

OD4: Fujisawa, H. et al.: "An 8.4ns Column-Access 1.3Gb/s/pin DDR3 SDRAM with an 8:4 Multiplexed Data-Transfer Scheme", 2006 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pages 557-566, IEEE Service Center, Piscataway, NJ, US, 6 to 9 February 2006.

III. In the contested decision, the Opposition Division came to the conclusion that the subject-matter of claim 1 of a main request, filed at the oral proceedings on 19 January 2012 at 10:50, did not fulfil the requirements of Article 52(1) as it was not new within the meaning of Article 54(1) and (2) EPC over the disclosure of document OD1. Invoking Article 114(2) EPC, the Opposition Division decided to disregard an auxiliary request I filed at the oral proceedings at 15:10. Claim 1 of each one of further auxiliary requests I to III filed with the letter of

19 December 2011 was found to infringe Article 123(2) EPC.

IV. With the notice of appeal the appellant maintained the requests on which the appealed decision was based and "the auxiliary request filed at the oral proceedings" as auxiliary request IV. As a further auxiliary request, it requested that oral proceedings be held.

V. With the grounds of appeal the appellant submitted sets of claims according to a main request and auxiliary requests I to III. The claims of the main request were the same as those of the main request on which the appealed decision was based. Auxiliary request I corresponded to a large extent to the request filed during oral proceedings before the Opposition Division at 15:10, claim 1 being the same. Auxiliary requests II and III essentially introduced additional limitations taken from dependent claims and corresponding to respective limitations of auxiliary requests II and III considered in the decision under appeal.

The appellant provided arguments in support of novelty of the subject-matter of claim 1 of the main request over the disclosure of each one of documents OD1, OD2 and OD3, and of claim 7 over document OD4, in order to address the grounds of the decision under appeal and preliminary objections raised in the first instance proceedings. With regard to auxiliary request I, the appellant indicated a basis in the application as originally filed for the additional features of claim 1 when compared with the main request. The appellant submitted further arguments in support of novelty of the subject-matter of claim 1 of each of auxiliary requests I to III over the disclosures of documents OD1 and OD2.

VI. Following a request by the then opponent/respondent of 6 August 2012, the EPO registered a change of its name to SK hynix Deutschland GmbH.

VII. With its reply, the then opponent (respondent) contended that the main request recited subject-matter extending beyond the content of the application as originally filed (pages 2 to 26 of its letter). Deficiencies with regard to added subject-matter were mentioned for each one of claims 1 to 8 of the main request (pages 17 to 26). The then respondent argued that auxiliary request I also infringed Article 123(2) EPC (pages 26 to 31) and that analogous deficiencies with respect to added subject-matter applied to auxiliary requests II and III, which merely combined features of claims of the higher ranking requests. Objections under Article 83 EPC were mentioned.

The then respondent further argued that none of the requests was patentable taking into account the relevant state of the art.

Regarding the main request, none of the claims was novel over document OD1 (pages 32 to 59). If the feature "sense amplifiers" was not considered to be disclosed in document OD1, the claimed subject-matter would not be inventive because it was "more than obvious" ("mehr als naheliegend") to include such a feature in the memory device of OD1. None of the claims was novel over document OD2 (pages 59 to 70). The subject-matter of each of the claims was either known from or not inventive over the disclosure of document OD3. The other prior-art documents cited in the opposition proceedings were still relevant.

Concerning the auxiliary requests (pages 83 to 94), the then respondent argued that none of the claims of auxiliary request I was inventive over the disclosure of document OD1. The same applied to the claims of auxiliary requests II and III, which merely combined features of the higher ranking requests.

VIII. With a letter dated 3 July 2013 the then respondent withdrew the opposition.

IX. The appellant was summoned to oral proceedings.

X. In response to the summons, the appellant informed the Board that it would not attend the oral proceedings. In the same letter, the appellant withdrew its auxiliary request pursuant to Article 116(1) EPC and requested a decision in accordance with the status of the file.

XI. In response, the Board cancelled the oral proceedings and informed the appellant that the decision would be given in writing.

XII. The appellant's final requests are that the patent be maintained in amended form on the basis of the claims according to the main request or one of auxiliary requests I to III.

XIII. Claim 1 of the main request reads as follows (itemisation added by the Board):

"A memory device (100) comprising:

(i) a storage array (135);

(ii) a column decoder (115) for addressing the storage array (135);

(iii) a read data buffer (163); and

(iv) a plurality of data lines (170) to communicate data between the storage array (13) and the read data buffer (163),

(v) wherein the read data buffer (163) is coupled to the storage array (135) via the data lines (170) and having control logic (169) to load data conveyed on all the data lines (170), while the storage array (135) is addressed by the column decoder (115), accessed in a column access operation and providing load data on all the data lines (170), into the read data buffer (163) in response to assertion of a load signal in a first prefetch mode;

characterized in that

(vi) the control logic (169) is further, while the storage array (135) is addressed by the column decoder (115), accessed in a column access operation and providing load data only on one of a plurality of address-selected strict subsets of all the data lines (170),

(vi.i) to select the strict subset of the data lines on which load data is provided (170) in response to an address value and to load data conveyed on the address-selected strict subset of the data lines (170) into the read data buffer (163) in response to assertion of the load signal in a second prefetch mode."

XIV. Claim 1 of auxiliary request I differs from that of the main request in that it further recites the following features itemised by the Board:

"(vii) wherein the storage array (135) comprises a set of sense amplifiers, active in both the first and second prefetch modes, to store data retrieved from selected storage cells within the storage array (135) and wherein the data

lines (170) are coupled between the read data buffer (163) and the set of sense amplifiers,

(viii) said column decoder (115) comprising column select circuits (333) each of which includes a column decoder (337) that decodes a column address to enable a corresponding one of column enable lines (338) and a plurality of sub-prefetch decoders (335), each corresponding to a respective column enable line (338) for activating one or more of a plurality of prefetch select-lines (325), according to a subprefetch address when the corresponding column enable line (338) is enabled such that load data is provided on data lines (170) according to the activated prefetch select lines (325)."

XV. Claim 1 of auxiliary request II differs from that of auxiliary request I in that in feature (viii) "according to a subprefetch address" was amended to "according to a prefetch address" and in that it further recites the following features:

"further comprising column decoding circuitry (115) to switchably connect all the data lines (170) to respective sense amplifiers within the set of sense amplifiers in the first prefetch mode and to switchably connect the address-selected strict subset of the data lines (170) to respective sense amplifiers within the set of sense amplifiers in the second prefetch mode."

XVI. Claim 1 of auxiliary request III adds to claim 1 of auxiliary request II the following feature:

"wherein the read data buffer (163) includes a plurality of storage elements to store read data, and wherein the control logic (169) includes multiplexer circuitry to switchably connect the

address-selected subset of the data lines (170) to a subset of the plurality of storage elements in the second prefetch mode, further comprising a programmable register to store a value that establishes either the first prefetch mode or the second prefetch mode within the memory device (100)."

XVII. The appellant's and the former opponent's arguments relevant to this decision are discussed in detail below.

Reasons for the Decision

1. The appeal complies with the provisions referred to in Rule 101 EPC and is therefore admissible.

The invention

2. The invention concerns a dynamic random access memory (DRAM) device to support scaled prefetch modes (see paragraph [0009] of the published patent).

2.1 The description of the patent explains that "[s]ignaling rate advances continue to outpace core access time improvement in dynamic random access memories (DRAMs), leading to device architectures that prefetch ever larger amounts of data from the core to meet peak data transfer rates". However, that "may result in retrieval of a substantial amount of unneeded data, wasting power and increasing thermal loading". Proposed DRAM architectures that output only a selected portion of prefetched data did not solve that problem, since they "generally prefetch an amount of data that corresponds to the maximum prefetch size, completely

filling a data buffer in the prefetch operation, then outputting only a portion of the buffered data" (paragraph [0002]).

2.2 The present invention relies on scaled prefetch modes, including a full prefetch mode and a partial prefetch mode.

In a full prefetch mode, an amount of data that corresponds to a maximum prefetch size is retrieved from the memory core and stored in a read data buffer before being transmitted (paragraph [0008], first five lines).

In a partial prefetch mode, an amount of data that corresponds to a fraction of the maximum prefetch size is retrieved from the memory core and stored in the read data buffer before transmission. In this mode, according to the description in paragraph [0008], "selected signal lines within the internal data path between the memory core and the read data buffer need not be driven and selected storage elements within the read data buffer need not be loaded", leading to "substantial power savings". Further power may be saved during write operations by driving only a subset of the signal lines of the internal data path with write data.

2.3 According to the invention as described in the patent specification, the memory core of the device includes a storage array formed by multiple independently addressable banks of storage cells, each of which including multiple sub-banks. Each of the sub-banks includes storage cells arranged in rows and columns, with word lines coupled to each row of storage cells and bit lines coupled to each column of storage cells. Each sub-bank additionally includes a set of sense

amplifiers coupled to the bit lines, the set of sense amplifiers for each bank of storage cells constituting a sense-amplifier bank (paragraphs [0013] and [0031], Figures 1 and 8).

2.4 The description further explains that the memory device receives requests from a control device, e.g. a memory controller external to the memory device (paragraph [0010]). Each incoming request includes an operation code indicating the nature of the requested operation, e.g. row activation, column read, column write, precharge, register write or refresh (see paragraph [0011]). A row activation request includes a row address and a bank address. During a row activation, the content of the activated row of storage cells with the given row address at the selected bank is transferred to a corresponding set of sense amplifiers (paragraph [0014]). After that, a column access operation may be directed to the activated row to read or write data at selected column locations within the sense amplifiers of the address-selected bank (paragraph [0015]). As explained in paragraph [0017], for one embodiment "the number of sense amplifiers accessed in a column access operation (i.e., a read or write operation) is determined according to the prefetch mode and may range from a full column of sense amplifiers, when a full prefetch mode is selected, to one or more fractions of a full column of sense amplifiers when one or more partial prefetch modes are selected".

Main request

3. Claim 1 of the main request recites a memory device comprising features (i) to (vi.i) listed in section XIII above.

3.1 Features (i) to (iv) specify basic components of the memory device, namely a storage array, a column decoder, a read data buffer, and a plurality of data lines to communicate data between the storage array and the read data buffer.

3.2 The "read data buffer (163)" (see Figure 2) implements the read data pipe 109 of Figure 1 (see paragraph [0019] of the patent publication). It loads the data read from an addressed location of the storage array. The first part of feature (v) further specifies that the read data buffer is coupled to the storage array and includes control logic. The control logic controls how data conveyed on the data lines is loaded into the read data buffer.

Features (v) to (vi.i) define the memory device, in particular the control logic of the read data buffer and the column decoder, in terms of its functionality during a column access operation (see point 2.4 above) in the two modes of operation, the "first prefetch mode" corresponding to a full prefetch mode (feature (v)) and the "second prefetch mode" corresponding to a partial prefetch mode (features (vi) and (vi.i)).

3.2.1 According to feature (v), during a column access operation in the first (full) prefetch mode, the column decoder addresses the storage array and provides load data on all the data lines, and the control logic loads data conveyed in all the data lines into the read data buffer in response to a load signal.

3.2.2 Features (vi) and (vi.i) recite that, during a column access operation in the second (partial) prefetch mode, the column decoder addresses the storage array, which

provides load data on one of a plurality of address-selected strict subsets of all the data lines. The control logic selects the strict subset of the data lines on which load data is provided "in response to an address value" and loads data conveyed on the address-selected strict subset of the data lines into the read data buffer in response to a load signal.

The "address value" of the claim is therefore a value identifying the "address-selected strict subset" in the partial prefetch mode during the column access operation. The description does not explicitly mention an "address value" in connection with the retrieval of strict subsets. However, paragraph [0023] refers to the strict subsets as "fractions" of the signal lines, and explains that the "subprefetch address signals (SPA) are used to identify (or select) the subset of core access signal lines used to convey read data" (see also paragraph [0025] and Figures 2 to 4).

4. *Novelty - claim 1*

4.1 The Opposition Division decided that the main request lacked novelty over document OD1. That document discloses a memory device, more concretely a dual data rate (DDR) synchronous DRAM (SDRAM) device, capable of operating in two modes "DDR1" and "DDR2" (see paragraph [0016]). In the DDR1 mode of operation, "2 bits are pre-fetched during data input/output operation so that a burst length of data is 2" or "two data are simultaneously ... outputted from the memory cell array". In the DDR2 mode, 4 bits are pre-fetched during data input/output operation or "four data are simultaneously ... outputted from the memory cell array". The device of document OD1 also supports two

sub-modes of DDR1, which are called DDR1-1 and DDR1-2 (paragraphs [0018], [0081] and [0082]).

Document OD1 therefore discloses a memory device with two modes of operation like those of the claimed invention. The DDR2 and DDR1 modes of document OD1 correspond respectively to the first (full) prefetch mode and second (partial) prefetch mode mentioned in the claim.

4.1.1 The memory device of OD1 is shown in Figure 1 (paragraph [0062]). It comprises a core section 500, corresponding to the storage array of the present claim, the core section including four memory cell arrays (paragraph [0081]). The memory device also comprises a column decoder 470 for addressing the core section, which activates and deactivates column selection lines (paragraphs [0077] and [0078]). Data is transferred between the memory cell array of the core section 500 and local data lines by means of the activated column selection lines (paragraph [0080]). The core section is connected to an output control circuit 700 by a plurality of global data lines GIO_E0, GIO_O0, GIO_E1 and GIO_O1. A memory cell array is connected to (or disconnected from) a local data line by a column selection line. The local data line is also connected to (or disconnected from) the global data line (paragraphs [0081] to [0082]). The device of document OD1 therefore comprises a storage array and a column decoder as recited in features (i) and (ii) of the claim, the storage array being "addressed by the column decoder [...] in a column access operation" as described in features (v).

4.1.2 The output control circuit 700 includes an output ordering circuit 710, an output data latch/mux 730, an

output buffer 750 and an output driver 770 (Figure 1, paragraph [0089]). The output control circuit and the output data latch/mux receive control signals including the PDDR2 signal which activates the DDR2 mode of operation (Figure 1, paragraph [0063]).

The output ordering circuit 710 and the output data latch/mux 730 are shown in more detail in Figure 12A. The output ordering circuit 710 comprises four output ordering parts 732, 734, 736 and 738 (see paragraphs [0089], [0090] and paragraph [0297]), receives the data from the global data lines GIO_E0, GIO_O0, GIO_E1 and GIO_O1 and activates some or all of its four output lines FDO (FDO_F0, FDO_S0, FDO_F1, FDO_S1), depending on which mode is selected (paragraphs [0090] and [0297], Figures 1 and 12A).

As explained in paragraph [0297], "[t]he output of the output ordering circuit 710 is provided to the output data latch/mux 730 via the FDO lines". The output data latch/mux 730 thus loads the data conveyed on the data lines FDO (see also Figure 12A, paragraph [0296]).

The Board therefore concludes, in line with the contested decision, that the combination of the output ordering circuit 710 and the data latch/mux 730 is a "read data buffer" as recited in feature (iii) of the claim. The global data lines of OD1 correspond to the plurality of data lines recited in feature (iv).

4.2 The output ordering circuit 710 and the output data latch/mux 730 receive the mode selection signal PDDR2 and column address signals CA0 and CA1 (Figure 1, paragraphs [0024] and [0063]).

Those signals are interpreted by the logic in those components to control their operation to "load data conveyed on all the data lines" in response to a load signal in the first prefetch mode DDR2, and to select a subset of the data lines in response to the load signal in a second prefetch mode DDR1 (paragraphs [0089] and [0090]).

In particular, the output ordering circuit 710 selectively activates lines FRT0 to FRT3 (of the four parts) of the output ordering circuit 710 on the basis of the least and most significant column addresses CA0 and CA1 (paragraphs [0024], [0271] to [0276], Figure 11A).

Lines FRT0 to FRT3 (of the four parts) of the output ordering circuit 710 are then used to selectively activate the output lines FDO of that circuit. In the DDR2 mode operation, all of the lines FDO_F0, FDO_S0, FDO_F1, and FDO_S1 are activated, and are selected by the output ordering parts 732, 734, 736 and 738 to direct data to the data latch/mux (paragraph [0306], Figure 12A). The combination of the output ordering circuit 710 and the data latch/mux 730 therefore also includes control logic as recited in features (v) of the claim.

In the DDR1 mode, the control lines FRT0 to FRT3 are used to select different subsets of data lines on which load data is provided (see paragraphs [0024], [0089] and [0090], Figure 12A, paragraph [0302]). For example, in the DDR1-1 mode when CA0 and CA1 have low levels, the first output ordering part 732 outputs the data of the global data line GIO_E0 to the FDO_F0 line via the DE01 line, and the second output ordering part 734 outputs the data of the global data line

GIO_O0 to the FDO_S0 line via the DO01 line. Since the lines FDO_F1 and FDO_S1 are not activated, the third and fourth output ordering parts 736 and 738 cannot output data to the lines FDO_F1 and FDO_S1 and the output data latch/mux 730 cannot receive the data through those FDO lines (paragraph [0302], Figure 12A). If CA0 has a high level and CA1 has a low level, the second output ordering part 734 outputs the data of the global data line GIO_O0 to the FDO_F0, and the third output ordering part 736 outputs the data of the global data line GIO_E1 to the FDO_S0 line. The lines FDO_F1 and FDO_S1 are not activated (paragraph [0303]).

Consequently, a strict subset of data lines is selected in response to the address value given by the column addresses CA0 and CA1 (paragraphs [0087] and [0302], Figure 1).

The Board therefore concludes that the logic of the output ordering circuit 710 and data latch/mux 730 of document OD1 is also configured to "select the strict subset of the data lines ... in response to an address value and to load data conveyed on the address-selected strict subset of the data lines ... into the read data buffer" in response to the load signal in a second prefetch mode DDR1, as defined in features (vi.i) of claim 1 of the main request.

4.3 In the grounds of appeal the appellant argued that the decision heavily relied on a particular interpretation of the claim language relating to the storage array and the column decoder. The memory device of document OD1 did not include feature (vi) and did not perform selective loading, feature (vi.i), which had the advantage of reducing power consumption.

4.3.1 According to the appellant, the Opposition Division had seen the DDR1 mode as loading less data than the DDR2 mode merely because some of the data loaded into the ordering circuits was not "current". The recited control-logic functions in the Opposition Division's interpretation were fully met by the operation of the storage array/column decoder, without the control logic performing any other action.

However, the correct interpretation was that the claim required an active selection of the strict subset of the data lines on which load data was provided rather than a "sensing" of data on all of the data lines whether they were active or not, as described in OD1, followed by a "reordering circuit" that worked on what was sensed on all data lines to place the valid sensed data ahead of the invalid sensed data.

The device of OD1 functioned without the selective loading of feature (vi.i) by using a different, switch-fabric-like technique where the four GIO lines from Figure 12A were all loaded into respective, identical ordering circuits ORD1 to ORD4 and switched onto four FD lines. But under the former opponent's construction, no inquiry into the OD1 ordering circuit operation was required. The readout circuit of OD1 thus sampled the data on the GIO lines without any control logic performing a selective loading from a strict subset of the data lines as defined in limiting feature (vi.i).

This difference had the advantage in the present invention that the data lines that were not address-selected were not loaded into anything: in the partial prefetch mode the unused load control multiplexers were configured to hold the data they already contained, and not to load anything, thus saving power.

4.3.2 The Board does not find those arguments persuasive. The core section of the device of OD1 includes four cell arrays EVEN0, ODD0, EVEN1, and ODD1 (Figure 5A, paragraph [0152]). The column decoder is explained in paragraph [0077] as follows:

> "The column decoder 470 is coupled to an output line DCAi of the column predecoder 450 and decodes the column address CAi. For example, the column decoder 470 includes four decoding blocks, and each of the decoding blocks may include two sub-decoding blocks. Output lines of each of the decoding blocks are coupled to a plurality of column selection lines CSL. The column selection lines are divided into CSL_E0, CSL_O0, CSL_E1 and CSL_O1 respectively corresponding to each of the four decoding blocks. The column decoder 470 disregards the column address output of one or two DCA lines during decoding."

Paragraphs [0078] and [0079] then explain that, depending on the mode selection, either two or four column-selection lines are activated.

The core section receives the signals from the column-selection lines (Figure 1). As explained in paragraph [0162] "in the DDR1-1 operation mode, since two column selection lines are simultaneously activated based on the level of the column address CAi, one of GIO_E0 and GIO_E1 and one of GIO_O0 and GIO_O1 are simultaneously activated, and the data of the cell array are transferred to the activated global data lines". Consequently, when the core section is addressed by the column decoder in a column access operation, load data is provided on all, if in the DDR2 mode, or only on one of a plurality of address-selected

strict subsets of all the data lines, if in the DDR1 mode, as recited in the claim in features (v) and (vi).

4.4 The appellant also argued that the arguments brought forward by the former opponent and shared by the Opposition Division with respect to the storage array and the column decoder were inconsistent. A consistent reasoning would lead to the conclusion that feature (vi.i) was not disclosed in document OD1.

According to the appellant, if document OD1 disclosed a column decoder, composed of four decoding blocks, which altogether addressed the storage array as a whole, then document OD1 failed to disclose claim feature (vi.i), since only parts of the decoder addressed parts of the storage array in the second prefetch mode.

4.4.1 The Board cannot follow this argument. Even if only parts of the decoder address parts of the core section, it is still the case that the column decoder as a whole addresses the core section, which corresponds to the storage array of the claim. The language of the claim covers such an embodiment. Feature (vi.i) is therefore also disclosed in document OD1 as explained under point 4.2 above.

4.5 In view of the reasoning under points 4.1 to 4.4.1 above, the Board concludes that the memory device of OD1 comprises all the features of the claim.

The subject-matter of claim 1 of the main request is therefore not new over document OD1 (Article 54(1) and (2) EPC).

Auxiliary request I

5. Claim 1 of auxiliary request I differs from claim 1 of the main request in that it further specifies features (vii) and (viii) (see section XIV above).

6. Features (vii) correspond to the features of claim 2 of the main request. According to the appellant, the additional features of auxiliary request I were based on original claim 2, page 23, lines 2 to 16 of the international publication and paragraph [0031] of the patent specification (corresponding to paragraph [0028] of the international publication).

Claims 1 to 5 and 7 of auxiliary request I are the same as the respective claims of the request filed during oral proceedings before the Opposition Division at 15:10, which was not admitted into the proceedings. Auxiliary request I differs from that previous request only in that some features corresponding to features of claim 1 were added to claim 6.

7. *Admission*

7.1 The Opposition Division did not admit into the proceedings the auxiliary request submitted during oral proceedings at 15:10, which substantially corresponds to auxiliary request I filed with the grounds of appeal. It is therefore questionable whether auxiliary request I should be admitted into the appeal proceedings.

7.2 The Opposition Division did not admit the request submitted during oral proceedings at 15:10 under Article 114(2) EPC, "for being facts not submitted in due time". In the decision under appeal it argued that

three late-filed requests had already been admitted during the oral proceedings. It shared the opponent's view that the opponent/respondent could not reasonably be expected to familiarise itself, in the time available, with the proposed amendments, which were "much more extensive than the previous ones, technically complex" and which "would require an additional search of relevant documents if the question of inventive step would arise" because they were "not based on any of the previous claims". The opponent had stated that a prolonged adjournment of the further proceedings would probably be necessary, if the amended claims of the proprietor’s request were to be admitted.

The decision under appeal also mentions that the subject of the proceedings had not changed since the summons, so that the proprietor had had the opportunity to file the amendments in due time. Furthermore, the amendments had not revealed that they would *prima facie* render the claims allowable with respect to added subject-matter or inventive step.

7.3 In the opinion of the Board, claims are not facts within the meaning of Article 114(2) EPC (see also Bühler in Singer/Stauder, "Europäisches Patentübereinkommen", 7th edition, 2016, Art 114, 52; T 133/92 of 18 October 1994, reasons 7), so that the Opposition Division did not provide the correct legal basis for not admitting the request. Nonetheless, the same reasoning would apply under Rule 116(2) EPC.

7.4 According to decision G 7/93 (OJ EPO 1994, 775) and established case law, a board of appeal should only overrule the way in which a first-instance department has exercised its discretion if it comes to the conclusion either that the first-instance department

has not exercised its discretion in accordance with the right principles or that it has exercised it in an unreasonable way (G 7/93, reasons 2.6). In a plurality of decisions the boards of appeal have stated that in such a case the board of appeal had nevertheless to exercise its discretion under Article 12(4) RPBA independently, giving due consideration to the appellant's additional submissions. In doing so, the board of appeal was not re-exercising the discretion of the department of first instance based on the case as it was presented then, but rather taking into account additional facts and different circumstances while exercising its own discretion under Article 12(4) RPBA (see e.g. T 971/11 of 4 March 2016, reasons 1.2, and T 2219/10 of 6 September 2016, reasons 3.1 to 3.3).

In line with those decisions, in the following the Board exercises its discretion with regard to auxiliary request I in the light of the new circumstances and submissions, while taking into account the reasoning given by the Opposition Division for not admitting the very similar request in the first instance proceedings.

7.5 The appellant did not provide arguments directly addressing the question why auxiliary request I should be admitted in the appeal proceedings. However, it provided a basis for the claim features and extensive arguments regarding novelty.

7.6 The Board notes that most of the reasons invoked by the Opposition Division no longer apply.

Since auxiliary request I was submitted with the grounds of appeal, both the Board and the former opponent have had time to examine the request. Moreover, the former opponent did not reiterate its

request that auxiliary request I not be admitted in appeal proceedings and has anyway withdrawn its opposition.

7.7 Exercising its discretion within the meaning of Article 12(4) RPBA, the Board therefore decides to admit the request into the appeal proceedings.

8. *Interpretation of claim 1*

8.1 Claim 1 of auxiliary request I includes the features "column decoder (115)" and "column decoder (337)". The column decoder 115 is depicted in Figure 1 and mentioned for instance in paragraphs [0009] and [0012] of the published patent (paragraphs [0006] and [0009] of the international publication of the application). In the Board's understanding, the column decoder 301 of Figure 8 (see below), which is described in paragraph [0031] of the patent (paragraph [0028] of the international publication extending through pages 22 to 25), is one possible implementation of the column decoder 115 of Figure 1. It is clear from that paragraph and Figure 8 that the feature "column decoder (337)" of the claim refers to the column-address decoder 337 (see also page 23, line 9, of the international publication).

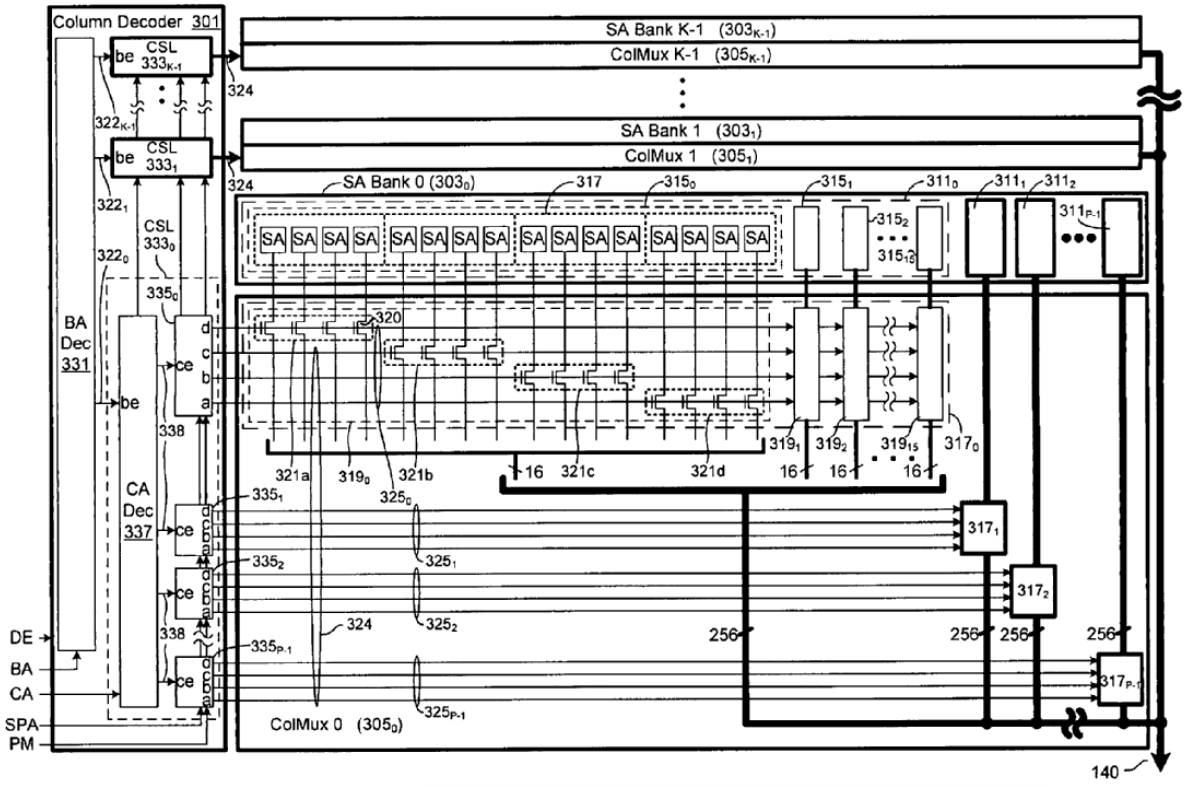
9. *Added subject-matter - claim 1*

9.1 The former opponent argued that claim 1 of auxiliary request I infringed Article 123(2) EPC because it did not include further essential features such as the functional elements and connection lines of the embodiment of Figure 8.

Features (viii) specify that said column decoder (115) comprises (itemisation added by the Board)
(a) column select circuits (333), each of which including
(a.1) a column address decoder (337) that decodes a column address to enable a corresponding one of column enable lines (338) and
(a.2) a plurality of sub-prefetch decoders (335),
(a.2.1) each corresponding to a respective column enable line (338)
(a.2.2) for activating one or more of a plurality of prefetch select-lines (325), according to a sub-prefetch address when the corresponding column enable line (338) is enabled
(a.2.3) such that load data is provided on data lines (170) according to the activated prefetch select lines (325).

9.1.1 According to paragraph [0028] (paragraph [0031] of the patent publication), "Figure 8 illustrates embodiments of a column decoder 301 and column multiplexers 305_0-305_{K-1} (ColMux 0 - ColMux K-1) that may be used in the memory device of Figure 1". Figure 8 shown below depicts a column decoder 301 comprising column select circuits 333_i, each of which includes a column address decoder 337 and a plurality of sub-prefetch decoders 335_i. Each sub-prefetch decoder corresponds to a respective column enable line "ce" 338 for activating a plurality of prefetch select-lines 325_i. These are the hardware elements of the memory device described in features (viii). As explained on page 23, lines 8 to 11, the column address decoder 337 decodes a column address to enable a corresponding one of column enable lines 338, so that feature (a.1) is disclosed in the original application.

FIG. 8



It is also clear from paragraph [0028], page 23, lines 14 to 16, that the sub-prefetch decoders 335 activate one or more of a plurality of prefetch select-lines 325_i, according to a sub-prefetch address when the corresponding column enable line 338 is enabled, for the purpose of providing load data to data lines 140 of Figure 8 (i.e. data lines 170 of Figure 1) according to the activated prefetch select lines 325_i, as recited in features (a.2.1) to (a.2.3). Each of features (viii) is thus described in the application with respect to the embodiment of paragraph [0028] and Figure 8.

9.2 That embodiment, however, includes many other features which are not specified in the claim, for example

- signal lines from request logic 105 (illustrated in Figure 1): decode enable DE, bank address BA,

column address CA, sub-prefetch address SPA, prefetch mode PM;

- bank address decode logic BA Dec 331, which "decodes the bank address to activate the bank-address-specified one of K bank enable lines 322_0-322_{k-1} that are coupled respectively to bank-enable inputs (be) of column select logic circuits 333_0-333_{K-1}" (page 23, lines 2 to 8);
- bank enable lines 322_i connecting elements 331 and 333_i;
- sense amplifier SA banks 303_0 to 303_{K-1};
- column multiplexers ColMux 305_0 to 305_{K-1}.

The memory device of claim 1 of auxiliary request I hence recites a combination of a generalised embodiment according to an original claim and features of the specific embodiment of Figure 8.

In order to answer the question of whether the claim fulfils the requirements of Article 123(2) EPC, it has to be established whether the claimed combination of features constitutes an allowable intermediate generalisation. According to the established case law, that amounts to determining whether the skilled person could recognise immediately that the features of the embodiment which have been included in the claim are not inextricably linked in terms of a functional or structural relationship to the other features of the particular embodiment.

9.3 In the present case, the architecture of column decoder 301 (115 of Figure 1) depicted in Figure 8 is especially designed to work with storage banks (page 22, first six lines of paragraph [0028]).

The sense amplifiers 303 are divided into banks (SA banks), each bank being associated with one column multiplexer 305_i. As explained in paragraphs [0011] and [0012], during a row activation operation the request logic 105 provides a bank address (BA) and row address (RA) to the row decoder 113, and a particular storage bank 131 (having an associated SA bank 303_i in Figure 8) is selected for row activation. The column access operation is directed to the activated row of the address-selected bank.

In the embodiment of Figure 8, each column select circuit CSL 333_i and column-address decoder 337_i work for a particular bank 131_i of the storage array, the bank comprising a column multiplexer ColMux 305_i and respective SA Bank 303_i. Each CSL 333_i is connected to the respective ColMux 305_i and is activated by a bank enable signal "be" from the bank address decode logic BA Dec 331 ("be" and BA Dec not being specified in the claim).

The column select circuits CSL 333_i and column address decoders CA Decs 337_i are only disclosed in the original application in the context of the column decoder of Figure 8 described in paragraph [0028]. As explained above, in that context the CSLs 333_i and CA Decs 337_i are especially conceived to work with a bank address decoder BA Dec 331 and storage banks. Since claim 1 of auxiliary request 1 mentions column select circuits CSLs 333_i and column-address decoders CA Decs 337_i but not storage banks, or any features concerning storage banks, it cannot be considered to be supported by the description of the embodiment of Figure 8 in the application as originally filed.

9.4 The Board further notes that the features left out cannot be implicitly understood from the claim either. As pointed out by the former opponent, the claim covers embodiments in which the storage array has different arrangements and the column select circuits CSL 333_i and column address decoders CA Decs 337_i have different functions than those disclosed in the application as originally filed.

9.5 Claim 1 of auxiliary request I therefore does not fulfil the requirements of Article 123(2) EPC.

Auxiliary requests II and III

10. Claim 1 of auxiliary request II (see section XV above) additionally recites features essentially describing column decoding circuitry (115) to switchably connect data lines (170) to respective sense amplifiers in each of the prefetch modes.

Claim 1 of auxiliary request III (see section XVI above) further describes features of the read data buffer 163 and of the control logic 169 of the read data buffer (see also Figure 2).

11. Claim 1 of either one of auxiliary requests II and III recites features (viii) of auxiliary request I without adding any of the features concerning storage banks. The reasoning given under point 9 above with regard to auxiliary request I therefore equally applies to claim 1 of auxiliary requests II and III.

12. From the above, the Board concludes that auxiliary requests II and III infringe Article 123(2) EPC.

Conclusion

13. Since none of the appellant's requests is allowable, the appeal is to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

I. Aperribay R. Moufang

Decision electronically authenticated