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Datasheet for the decision
of 11 July 2017

Case Number: T 0871/12 - 3.4.03

Application Number: 01480078.3

Publication Number: 1209725

IPC: H01L21/02, H01L23/522, H01L23/528, H01L23/532, H01L23/60, H01L27/06, H01L27/08

Language of the proceedings: EN

Title of invention:
High performance system-on-chip using post passivation process

Applicant:
QUALCOMM Incorporated

Headword:

Relevant legal provisions:
EPC Art. 123(2)

Keyword:
Amendments - added subject-matter (yes)

Decisions cited:

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It can be changed at any time and without notice.

Catchword:

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Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 0871/12 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 11 July 2017

Appellant: QUALCOMM Incorporated
(Applicant) 5775 Morehouse Drive
San Diego, CA 92121 (US)

Representative: Schmidbauer, Andreas Konrad
Wagner & Geyer Partnerschaft
Patent- und Rechtsanwälte
Gewürzmühlstrasse 5
80538 München (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted on 7 November 2011 refusing European patent application No. 01480078.3 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman G. Eliasson
Members: T. M. Häusser
C. Schmidt

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division refusing the European patent application No. 01480078 for lack of inventive step (Article 56 EPC 1973).

II. Oral proceedings before the board took place in the absence of the appellant, of which the board had been informed beforehand.

The appellant had requested in writing that the decision under appeal be set aside and that the patent be granted on the basis of the main request filed with letter dated 7 March 2012 or on the basis of the first auxiliary request filed with letter dated 17 September 2011 and forming the basis of the decision under appeal.

III. In a communication pursuant to Article 15(1) RPBA the board expressed *inter alia* its provisional opinion that the claims of both requests contained subject-matter going beyond the application as filed, contrary to the requirements of Article 123(2) EPC.

IV. The wording of independent claim 1 of the main and auxiliary request is as follows (board's labelling "(a)" to "(i)"):

Main request:

"1. An integrated circuit chip comprising:
- a silicon substrate (10);
- multiple semiconductor devices (11) in or on said silicon substrate, wherein said multiple semiconductor devices comprise a transistor;

- a first dielectric layer (14) over said silicon substrate (10);

(a) - a metallization structure (13, 16) over said first dielectric layer (14), wherein said metallization structure comprises a first metal layer (13) and a second metal layer (13, 16) over said first metal layer, wherein said metallization structure (13, 16) comprises electroplated copper;

(b) - a second dielectric layer (14) between said first and second metal layers;

(c) - a passivation layer (18) over said metallization structure (13, 16) and over said first and second dielectric layers (14), wherein a first opening in said passivation layer (18) is over a first contact point (16) of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer (18) is over a second contact point (16) of said metallization structure, and said second contact point is at a bottom of said second opening, wherein said passivation layer comprises a nitride layer;

(d) - a first polymer layer (20) on said passivation layer (18), wherein a third opening in said first polymer layer is over said first contact point (16), and a fourth opening in said first polymer layer is over said second contact point (16), wherein said first polymer layer (20) has a thickness between 2 and 150 micrometers;

(e) - a coil (40) directly over said first polymer layer (20), wherein said coil (40) is connected to said first contact point (16) through said third opening, wherein said coil (40) comprises electroplated copper;

(f) - a metal line (26) directly over said first polymer layer (20) and separately located from said

coil (40), wherein said metal line (26) is connected to said second contact point (16) through said fourth opening; and

(g) - a second polymer layer over said metal line (26)."

Auxiliary request:

Claim 1 of the auxiliary request differs from claim 1 of the main request in that features (e) and (f) are replaced by the following features (h) and (i), respectively:

(h) - a coil (40) ~~directly~~ over said first polymer layer (20), wherein said coil (40) is connected to said first contact point (16) through said third opening, wherein said coil (40) comprises electro-plated copper;

(i) - a metal line (26) ~~directly~~ over said first polymer layer (20) ~~and separately located from said coil (40)~~, wherein said metal line (26) is connected to said second contact point (16) through said fourth opening; and

V. In response to the objection of added subject-matter raised in the board's communication pursuant to Article 15(1) RPBA the appellant made no submissions and merely stated that it would not attend the oral proceedings before the board.

Reasons for the Decision

1. Main request - amendments

1.1 The subject-matter of claim 1 underlying the decision was deemed by the examining division to lack inventive step (see points 9 and 11 of the Reasons of the decision). The decision contains no objection under Article 123(2) EPC against that claim.

However, the board is of the opinion that the subject-matter of claim 1 of the main request, which had been further amended with the letter setting out the grounds of appeal resulting in a somewhat narrower scope (see point IV. above), extends beyond the content of the application as filed.

1.2 Claim 1 of the main request relates to the subject-matter of original independent claim 28 as well as Figures 2 to 4 and the corresponding parts of the description of the application, which relate to the integrated circuit chip comprising an inductor formed on the surface of a polymer layer.

1.2.1 Compared to original independent claim 28 it has been omitted in claim 1 of the main request that

- the metallization structure (see features (a) and (b) of claim 1 of the main request) is an "overlaying interconnecting metal[l]ization structure comprising one or more layers of interconnects over the active surface of said substrate, said layers of interconnects comprising conductive interconnect lines or conductive contact points or conductive vias in one or more layers",
- the contact points of the metallization structure (see feature (c) of claim 1 of the main request) are "provided in or on the surface of said overlaying interconnecting metal[l]ization structure, at least one of said points of electrical contact making contact with at least one of said conductive

interconnect lines or said conductive contact points or said conductive vias provided in said one or more layers of said overlaying interconnecting metal[l]ization structure, at least one of said metal lines or said contact points or said conductive vias making contact with at least one of said points of electrical contact provided to said semiconductor devices in or on the surface of said substrate",

- the openings in the passivation layer and in the first polymer layer (see features (c) and (d) of claim 1 of the main request) are "filled with a conductive material, creating metal contacts through said openings",
- the first polymer layer (see feature (d) of claim 1 of the main request) is "substantially thicker than said passivation layer and that is also substantially thicker than an inter-layer dielectric used for creating said interconnecting metallization structure".

1.2.2 In the description of the application the following problems are mentioned in relation to creating inductors on the surface of a semiconductor substrate (see page 2, lines 21-30):

> "One of the problems that is encountered when creating an inductor on the surface of a semiconductor substrate is that the self-resonance that is caused by the parasitic capacitance between the (spiral) inductor and the underlying substrate will limit the use of the inductor at high frequencies. As part of the design of such an inductor it is therefore of importance to reduce the capacitive coupling between the created inductor and the underlying substrate.

At high frequencies, the electromagnetic field that is generated by the inductor induces eddy currents in the underlying silicon substrate."

Accordingly, it is stated that invention provides (see page 11, lines 3-15)

> "an Integrated Circuit structure where re-distribution and interconnect metal layers are created in layers of dielectric on the surface of a conventional IC. A layer of passivation is deposited over the dielectric of the re-distribution and interconnection metal layers, a thick layer of polymer is deposited over the surface of the layer of passivation. Under the present invention, a high-quality electrical component is created on the surface of the thick layer of polymer.
>
> The invention addresses, among others, the creation of an inductor whereby the emphasis is on creating an inductor of high Q value on the surface of a semiconductor substrate using methods and procedures that are well known in the art for the creation of semiconductor devices. The high quality of the inductor of the invention allows for the use of this inductor in high frequency applications while incurring minimum loss of power."

1.2.3 In the description of the application it has thus been presented as being part of the invention that an integrated device is provided comprising on the one hand the semiconductor devices and on the other hand the electrical component performing analog functions, connected to each other by the appropriate wiring. Indeed, it emerges from the description that nothing

other than such an integrated device is intended by the invention. Furthermore, in relation to the embodiment of an inductor on the surface of a polymer layer, it is crucial that the inductor is far removed from the underlying substrate in order to reduce both the capacitive coupling between the inductor and the substrate and the eddy currents induced in the substrate by the inductor. This is achieved by providing a polymer layer that is thick enough, i. e. substantially thicker than the passivation layer as well as an inter-layer dielectric used in the interconnecting metallization structure.

Therefore, the board considers that the omission of the four features mentioned above in claim 1 of the main request is not directly and unambiguously derivable from the application as filed.

1.3 According to feature (a) of claim 1 of the main request the claimed metallization structure "comprises electroplated copper".

In the application as filed it is disclosed that copper may be applied using electroplating to create the points of electrical contact provided in or on the surface of the metallization structure, to fill the openings in the passivation layer and the polymer layer, or to create the inductor (see original claim 35 and the original description, page 14, lines 24-33, and page 16, lines 15-29). However, there is no indication in the application as filed that the *metallization structure* comprises electroplated copper. Moreover, the skilled person would not consider this to be implicitly disclosed in the application documents, either.

Consequently, feature (a) of claim 1 of the main request introduces subject-matter into the claim which is not directly and unambiguously derivable from the application as filed.

1.4 In feature (c) of claim 1 of the main request it is specified that the passivation layer "comprises a nitride layer".

However, in the original application documents it is merely disclosed that the passivation layer may be formed of *silicon nitride* or of the *combination of plasma enhanced CVD (PECVD) oxide and PECVD nitride* (see original claim 30 and the original description, page 12, lines 7-9, and page 13, lines 30-33). Hence, the above formulation in feature (c) of claim 1 of the main request constitutes a generalization of the disclosed subject-matter which has no basis in the application as filed.

1.5 The above objections were raised in the board's communication pursuant to Article 15(1) RPBA annexed to the summons to attend oral proceedings before the board. The appellant made no further submissions in response to the communication and merely stated that it would not attend the oral proceedings.

After reconsidering the issues at the oral proceedings the board saw no reason to change its position expounded in the communication.

1.6 In view of the above the subject-matter of claim 1 of the main request extends beyond the content of the application as filed, contrary to the requirements of Article 123(2) EPC.

2. Auxiliary request - amendments

Claim 1 of the auxiliary request differs from claim 1 of the main request merely in that features (e) and (f) are replaced by features (h) and (i), resulting in a somewhat broader scope. Hence, the above objections of added subject-matter, which relate to the formulation of features (a) to (d), apply to claim 1 of the auxiliary request as well.

Consequently, the subject-matter of claim 1 of the auxiliary request extends beyond the content of the application as filed, contrary to the requirements of Article 123(2) EPC.

3. Conclusion

As the claims of the main request and of the auxiliary request do not meet the requirements of the EPC, the appeal has to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated