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Datasheet for the decision of 17 May 2018

Case Number: T 0661/12 - 3.5.04

Application Number: 10156790.7

Publication Number: 2244458

IPC: H04N5/08, H04N5/44, H04N17/04, H04N5/46

Language of the proceedings: EN

Title of invention:
Method and circuit for recovering the correct timing of a received analogue video signal

Applicant:
Vestel Elektronik Sanayi ve Ticaret A.S.

Headword:

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step - main and auxiliary requests (no)

Decisions cited:

Catchword:

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Boards of Appeal

Chambres de recours

Boards of Appeal of the
European Patent Office
Richard-Reitzner-Allee 8
85540 Haar
GERMANY
Tel. +49 (0)89 2399-0
Fax +49 (0)89 2399-4465

Case Number: T 0661/12 - 3.5.04

D E C I S I O N
of Technical Board of Appeal 3.5.04
of 17 May 2018

Appellant: (Applicant)	Vestel Elektronik Sanayi ve Ticaret A.S. Organize Sanayi Bölgesi 45030 Manisa (TR)
Representative:	Cayli, Hülya Paragon Consultancy Inc. Koza Sokak No: 63/2 GOP 06540 Ankara (TR)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 14 November 2011 refusing European patent application No. 10156790.7 pursuant to Article 97(2) EPC**

Composition of the Board:

Chairman	C. Kunzelmann
Members:	B. Willems
	G. Decker

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division dated 14 November 2011 refusing European patent application No. 10156790.7, published as EP 2 244 458 A1.

II. The documents cited in the decision under appeal included the following:

D1: EP 1 916 841 A2

D2: US 5 367 337 A

D3: US 2005/030426 A1.

III. The application was refused on the ground that the subject-matter of claim 1 of the sole request lacked novelty over the disclosure of document D1 (Article 54 EPC).

IV. The applicant filed notice of appeal, requesting that the examining division's decision be set aside. With its statement of grounds of appeal, the appellant filed amended claims in accordance with a main and an auxiliary request. It provided arguments as to why the amended claims met the requirements of Articles 54, 56 and 84 EPC.

V. The board issued a summons to oral proceedings. In a communication under Article 15(1) RPBA (Rules of Procedure of the Boards of Appeal, OJ 2007, 536) which was annexed to the summons, the board gave its provisional opinion that:

(a) claim 1 of both requests did not meet the requirements of Article 84 EPC;

(b) the subject-matter of claim 1 of both requests extended beyond the disclosure of the application as filed (Article 123(2) EPC); and

(c) the subject-matter of claim 1 of both requests lacked inventive step over the disclosure of D1 combined with the common general knowledge of the person skilled in the art (Article 56 EPC).

VI. With its reply dated 16 April 2018, the appellant filed amended claims according to a main request and first and second auxiliary requests, replacing the previous requests on file. It submitted arguments as to why the amended claims met the requirements of Articles 54, 56, 84 and 123(2) EPC.

VII. The board held oral proceedings on 17 May 2018. The appellant was represented. At the oral proceedings, the appellant withdrew its main request dated 16 April 2018. It requested that the decision under appeal be set aside and that a European patent be granted on the basis of the claims of the main request filed as first auxiliary request with the letter dated 16 April 2018 or of the auxiliary request filed as second auxiliary request with the letter dated 16 April 2018.

At the end of the oral proceedings, the chairman announced the board's decision.

VIII. Claim 1 of the main request reads as follows:

"Circuit for recovering a vertical timing and a horizontal timing of a received analogue video signal, comprising:

- means for measuring the vertical timing of the received analogue video signal by measuring the number of lines per field of the incoming analogue video signal;

characterized by

- means for measuring the horizontal timing of the received analogue video signal by measuring the number of pixels per line of the incoming analogue video signal, wherein the parameter pixel per horizontal line PPHL is measured as:

PPHL = fs/fh

wherein fs is the sampling frequency and fh is the horizontal frequency;

- means for determining video format of the received analogue video signal on the basis of the measured horizontal and vertical timing of the received analogue video signal, wherein said circuit further comprises means for adjusting scaling parameters for the received analogue video signal."

IX. Claim 1 of the auxiliary request reads as follows:

"Circuit for recovering a vertical timing and a horizontal timing of a received analogue video signal, comprising:

- means for measuring the vertical timing of the received analogue video signal by measuring the number of lines per field of the incoming analogue video signal;

characterized by

- means for measuring the horizontal timing of the received analogue video signal by measuring the number of pixels per line of the incoming analogue video signal, wherein the parameter pixel per horizontal line PPHL is measured as:

PPHL = fs/fh

wherein fs is the sampling frequency and fh is the horizontal frequency;

- means for determining video format of the received analogue video signal on the basis of the measured horizontal and vertical timing of the received analogue video signal, wherein said circuit further comprises means for adjusting scaling parameters for the received analogue video signal, so as to well fit displayed signal to display active area of said display device on the basis of said measured horizontal and vertical timing,

wherein the circuit further comprises:

- a circuit (2) for clamping said received analogue video signal,
- an analogue to digital converter for digitizing said clamped signal;
- a slicing circuit for slicing synchronization pulses comprised by the digitized signal;

- a circuit for measuring horizontal and vertical timings of the video signal received from the slicing circuit;
- a circuit for calculating scaling parameters based on the measured horizontal and vertical timings.
- a scaler (3), which has the function of scaling the video contents of the signal received from the slicing circuit in accordance with the scaling parameters."

X. The examining division argued that document D1 disclosed all features of claim 1 underlying the decision under appeal (see decision, Reasons, section 2).

XI. The appellant's arguments where relevant to the present decision may be summarised as follows:

(a) The claims of both requests specified that

"*the parameter pixel per horizontal line PPHL is measured as:*

PPHL = fs/fh

wherein fs is the sampling frequency and fh is the horizontal frequency".

Calculating the PPHL parameter rather than measuring the line length in terms of the sampling frequency "*realizes a precise measurement of the number of pixels per line [... and] is not disclosed in the prior art [... Hence] a skilled person does not find a hint for this solution in D1 and also not in D2 and D3*" (see reply dated 16 April 2018, page 3).

(b) Paragraph [0070] of D1 did not disclose adjusting scaling parameters for the received video signal (see statement of grounds of appeal, paragraph bridging pages 2 and 3). Paragraph [0003] of D1 related only to the background to D1 and mentioned that the number of pixels in a line could be different for different formats (see reply dated 16 April 2018, page 4, second and fourth paragraphs).

(c) In D1, only standard size formats of the video were identified, whereas the claimed apparatus supported a "*timing [which] is a nonstandard one, substantially within the area*" (see statement of grounds of appeal, page 3, penultimate paragraph). Calculating the line length rather than measuring the line length aided in coping with non-standard input signals.

(d) D1 did not disclose the circuit features of the implementation specified in claim 1 of the auxiliary request.

Reasons for the Decision

1. The appeal is admissible.

2. *Interpretation of claim 1 of both requests*

2.1 Claim 1 of both requests specifies "*adjusting scaling parameters for the received analogue video signal*".

2.2 The term "scaling parameters" is broad and could relate to any characteristic, such as the amplitude of the video signal.

2.3 Paragraph [0020] of the A1 publication of the application discloses that the scaler "*has the function of adjusting the video contents to the display panel resolution*". On the basis of this paragraph, the board interprets the feature quoted in point 2.1 to relate *inter alia* to adjusting the line length or line frequency to the resolution of the display. This interpretation is further supported by claim 1 of the auxiliary request, which specifies that the scaling parameters are adjusted "*so as to well fit displayed signal to display active area of said display device*".

3. *Main request - inventive step (Article 56 EPC)*

3.1 D1 is the closest prior art for the assessment of inventive step; it discloses a circuit for recovering a vertical timing and a horizontal timing of a received analogue video signal having the following combination of features:

means for measuring the horizontal timing of the received analogue video signal (see paragraph [0023]: "*the 'line length', which is a measure of the number of 108 MHz clock cycles required to display one line*" and paragraph [0063]: "*As shown in FIG 12, all counts can be measured in terms of sample counts*");

means for measuring the vertical timing of the received analogue video signal by measuring the number of lines per field of the incoming analogue video signal (see Figure 12 and paragraph [0063]: "*the number of lines per frame is determined by dividing flng by llng, i.e., lines_per_f = flng / llng*", where flng is the frame length and llng the line length);

means for determining the video format of the received analogue video signal on the basis of the measured horizontal and vertical timings of the received analogue video signal (see paragraph [0060]: "*Metrics that can be determined from the HSync and VSync pulses embedded within a CSync signal and that can later be used to identify uniquely a format [...] include [...] the Line Length; the number of Lines/Field*").

3.2 Paragraphs [0023] and [0030] of D1 disclose that "*the analog input signal is sampled at a clock rate of 108 MHz*", and according to paragraph [0063] "*all counts can be measured in terms of sample counts*". Hence, the metrics disclosed in document D1 are based on the sampling frequency, i.e. the number of 108 MHz clock cycles. In the present application, the PPHL parameter is likewise based on the sampling frequency (see paragraph [0014]: "*[with the] ADC of the video processor sampling the signals at 81 Mhz [...] the parameter PPHL 'pixel per horizontal line' (number of available sample[s] between two horizontal sync pulses) should be measured as:*
PPHL = fs/fh
where fs is the sampling frequency, fh is the horizontal frequency of the incoming signal").

3.3 Moreover, paragraph [0003] of D1 discloses that "*[k]nowing the frame frequency, line frequency and sample frequency are critical to (a) locking to the input signal and (b) generating an image with the proper resolution for each frame*". It is self-evident that the mentioned parameters are also "critical", i.e. need to be input to video decoder 110 to generate an output signal "*compatible [...] for display on the display device 104*" (see D1, paragraph [0022]). Thus, contrary to the appellant's opinion, the metrics

determined in D1 are input to the decoder to generate an image with the proper resolution, i.e. to adjust the scaling parameters for the received signal (see point XI(b) and section 2 above).

3.4 The board disagrees with the appellant's view that "*according to D1 only standard size formats of the video are identified*". Paragraphs [0062] and [0063] of D1 define tolerances for the metrics which allow a format to be identified even if the input "*timing is a nonstandard one, substantially within the area*" (see D1, paragraph [0076]: "*The first entry that describes the current metrics, within the defined tolerances, can be identified as the format of the analog input signal*", and point XI(c) above).

3.5 Thus, the subject-matter of claim 1 of the main request differs from the disclosure of D1 in that the former specifies that the horizontal timing is calculated from the ratio between the sampling frequency and the horizontal frequency (see formula quoted in point XI(a) above), whereas the latter discloses that the horizontal timing is measured as a number of sample counts (see point XI(a) above).

3.6 The technical effect resulting from this difference is that the line length is calculated rather than measured.

3.7 Therefore, the objective technical problem may be identified as how to provide an alternative manner of determining the line length in the metrics for identifying the format.

3.8 The board is of the opinion that it belongs to the common general knowledge of a person skilled in the art

that, in the context of the present application, calculating the line length on the basis of the sampling frequency is an alternative to measuring the line length on the basis of the sampling frequency. These options for determining the "timing" of an analogue video signal are also known from D1, which discloses measuring the line length and calculating the line number (see point 3.1 above).

3.9 The board has not been persuaded that calculating the line length from an 81 MHz sampling frequency is more precise than measuring the line length in terms of a 108 MHz sampling frequency (see point XI(a) above). Moreover, it has not been convinced by the mere assertion that calculating rather than measuring the samples in a line facilitates the processing of non-standard formats (see point XI(c) above).

3.10 In view of the above, the board concludes that the subject-matter of claim 1 of the main request lacks inventive step over the disclosure of D1 combined with the common general knowledge of a person skilled in the art (Article 56 EPC).

4. *Auxiliary request - inventive step (Article 56 EPC)*

4.1 In comparison with claim 1 of the main request, claim 1 of the auxiliary request further specifies features of the circuit for measuring the horizontal and vertical timings.

4.2 D1 demonstrates that these features are well-known elements of a circuit for extracting horizontal and vertical sync pulses.

D1 discloses clamping the analogue signal (see paragraph [0027]: "*the block 106 can normalize an offset of the input signal with a DC restore ('DCR') block 214*"), digitising the signal (see paragraph [0030]: "*when [...] the amplitude of the signal is digitized into 256 levels*") and passing the signal through a slicer (see paragraph [0027]: "*HSync and VSync pulses can be detected by passing the [...] signal though a [...] "Slicer" [...]. [M]etrics about the Sync pulses are extracted [...] and the format of the input signal can be determined in the format ID block 210 based on the extracted metrics*").

The measured horizontal and vertical timings are then input to the decoder to generate an image with a resolution compatible with the output device (see point 3.3 above).

4.3 The appellant did not contest this assessment of the disclosure of D1.

4.4 In view of the above, the board concludes that the subject-matter of claim 1 of the auxiliary request lacks inventive step over the disclosure of document D1 combined with the common general knowledge of a person skilled in the art (Article 56 EPC).

5. Since none of the appellant's requests is allowable, the appeal is to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

K. Boelicke C. Kunzelmann

Decision electronically authenticated