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Datasheet for the decision of 27 April 2016

Case Number: T 0200/12 - 3.5.02

Application Number: 09163916.1

Publication Number: 2107679

IPC: H03K19/003, H03K19/094

Language of the proceedings: EN

Title of invention:
Single-event-effect tolerant SOI-based logic device

Applicant:
Japan Aerospace Exploration Agency
High-Reliability Engineering & Components Corporation

Relevant legal provisions:
EPC Art. 114(2)
RPBA Art. 13(1)

Keyword:
Late-filed auxiliary requests - admitted (no)

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Case Number: T 0200/12 - 3.5.02

D E C I S I O N
of Technical Board of Appeal 3.5.02
of 27 April 2016

Appellant: (Applicant 1)	Japan Aerospace Exploration Agency 44-1, Jindaiji-Higashimachi 7-chome Chofu-shi, Tokyo 182-8522 (JP)
Appellant: (Applicant 2)	High-Reliability Engineering & Components Corporation No. 7 Yoshimura Bldg., Blue Box 8-1 Higashi-Arai Tsukuba-shi Ibaraki 305-0033 (JP)
Representative:	Desormiere, Pierre-Louis Cabinet Beau de Loménie 158, rue de l'Université 75340 Paris Cedex 07 (FR)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 30 August 2011 refusing European patent application No. 09163916.1 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	M. Léouffre
Members:	H. Bronold
	W. Ungler

Summary of Facts and Submissions

I. The appeal is directed against the decision of the examining division to refuse the patent application for lack of inventive step and inadmissible amendments.

II. In the written procedure and at the beginning of the oral proceedings, the appellants requested that the decision under appeal be set aside and that a patent be granted to them on the basis of the claims of one of their main request or on the basis of the claims of their first to third auxiliary requests, all filed together with the statement setting out the grounds of appeal.

III. The appellants also requested reimbursement of the appeal fee, without however identifying any substantial procedural violation by the examining division that would justify such reimbursement (Rule 103(1) EPC).

IV. During the oral proceedings the appellants withdrew the first to third auxiliary requests. They filed new fourth and fifth auxiliary requests and requested that the decision under appeal be set aside and a patent be granted to them on the basis of the claims of the fourth auxiliary request or, if that was not possible, on the basis of the claims of the fifth auxiliary request.

V. The following document cited in the proceedings before the examining division is relevant for this decision:

D2: XP011041840, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 47 no. 6,

ISSN:0018-9499, 01-12-2000, MARK P BAZE ET AL: "A Digital CMOS Design Technique for SEU Hardening"

VI. Claim 1 of the fourth auxiliary request reads as follows:

"A single-event-effect tolerant SOI-based 2-input NAND element (13) comprising:
a pair of a first p-channel MOS transistor (13P1) and a second p-channel MOS transistor (13P2) which have channels connected in parallel with each other; and
a pair of a first n-channel MOS transistor (13N1) and a second n-channel MOS transistor (13N2) which have channels connected in series with each other, wherein:
said p-channel MOS transistor pair (13P1, 13P2) and said n-channel MOS transistor pair (13N1, 13N2) are connected in series in a direction from a node connected to the side of a first voltage source to a node connected to the side of a second voltage source, and each transistor of said pairs (13P1, 13P2, 13N1, 13N2) is formed with its respective body (34) floated from a substrate (36) by an $Si0_2$ insulating film (35), the potential of the body varying depending on a voltage to be applied to the source, and depending on a voltage to be applied to the drain;
respective gates of said first p-channel MOS transistor (13P1) and said first n-channel MOS transistor (13N1) are connected to a first input (A);
respective gates of said second p-channel MOS transistor (13P2) and said second n-channel MOS transistor (13N2) are connected to a second input (B); and
a node between said p-channel MOS transistor pair (13P1, 13P2) and said n-channel MOS transistor pair (13N1, 13N2) is connected to an output (Y),

characterized in that said single-event-effect tolerant SOI-based 2-input NAND element (13) includes a double structure in which each of said first p-channel MOS transistor (13P1), said second p-channel MOS transistor (13P2), said first n-channel MOS transistor (l3Nl) and said second n-channel MOS transistor (13N2), is combined with an additional MOS transistor (13P3, 13P4, 13N3, l3N4) having a channel of the same conductive type as that thereof and a gate interconnected to a gate thereof, in such a manner that their channels are connected in series, the SOI-based element being configured to allow each of the transistors themselves as components to be less subject to SEE."

VII. Claim 1 of the fifth auxiliary request differs from claim 1 of the fourth auxiliary request in the following:

the expression
", and each transistor of said pairs (13P1, 13P2, 13N1, 13N2) is formed with its respective body (34) floated from a substrate (36) by an $Si0_2$ insulating film (35)"

was deleted from the preamble and the expression:
"and in that in said SOI-based element, a body is floated from a substrate by an SiO2 insulating film"

was added to the characterising portion and further in that the expression
"the potential of the body is varying depending on the voltage to be applied to the source, and depending on the voltage to be applied to the drain,"

was moved from the preamble to the characterising portion.

VIII. Both requests on file contain the feature

"the SOI-based element being configured to allow each of the transistors themselves as components to be less subject to SEE."

IX. The appellants essentially argued as follows:

The feature added to claim 1 of the fourth and fifth auxiliary requests was based on page 19, lines 4 and 5 of the originally filed description. Although this passage belonged to the embodiment of an inverter, the content of this passage also applied to the embodiment of the 2-input NAND element being claimed in claim 1 according to the fourth auxiliary request and according to the fifth auxiliary request. The amendment further contributed to establishing that the subject-matter of claim 1 refers to fully depleted SOI (Silicon On Insulator) technology in contrast to bulk technology or partially depleted SOI technology as disclosed in document D2.

Reasons for the Decision

1. Admissibility of the fourth and fifth auxiliary requests: Article 13(1) RPBA

1.1 According to the appellants, the feature added to claim 1 of the fourth and fifth auxiliary requests, that "the SOI-based element being configured to allow each of the transistors themselves as components to be less subject to SEE" is based on page 19, lines 4 and 5 of the originally filed description.

However, this passage of the originally filed description is part of the description of another embodiment, namely that of the inverter 3I shown in figure 4. For inverter 3I, the tolerance towards SEE (single event effect) is established by connecting node A (the node between two series connected p-channel transistors) with node B (the node between two series connected n-channel transistors), so that the potential difference between these nodes is approximately zero, see the description of the inverter 3I in the originally filed description from page 17, line 6.

The property described for inverter 3I, that the SOI-based element is configured to allow each of the transistors themselves as components to be less subject to SEE, therefore needs to be read in the context of the remainder of the description of inverter 3I, i.e. the connection between nodes A and B.

The original description does not however contain a similar passage defining a connection between nodes A and B with respect to the 2-input NAND element as claimed in claim 1 of the fourth and fifth auxiliary request. Therefore, the respective property of inverter 3I cannot be attributed to the 2-input NAND claimed in claim 1.

1.2 Consequently, the amendment made to claim 1 of the fourth and fifth auxiliary requests has no basis in the specification as originally filed. Thus, the added feature contravenes Article 123(2) EPC.

2. Even if the amendment were considered allowable, it would prima facie not be suitable to overcome the

objections as to lack of inventive step regarding the claimed subject matter.

It is a matter of course that logic circuits realised in SOI technology, regardless of whether they are realised in fully depleted SOI technology or in partially depleted SOI technology, are less subject to SEE than logic circuits realised in bulk technology. Thus, the amendment merely describes an inherent property of SOI technology which, as such, belongs to the common general knowledge of the person skilled in the art.

3. Therefore, the board exercises its discretion under Article 13(1) RPBA not to admit the fourth and fifth auxiliary requests into the procedure.

4. As there is no allowable request, it follows that the appeal must be dismissed.

5. Since the appeal is not allowable, the board is not in a position to order reimbursement of the appeal fee under Rule 103(1)(a) EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Léouffre

Decision electronically authenticated