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Datasheet for the decision of 22 November 2016

Case Number: T 0107/12 - 3.5.02

Application Number: 05789530.2

Publication Number: 1794883

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Language of the proceedings: EN

Title of invention:
Electronic filter device for the reception of TV-signals

Patent Proprietor:
Unitron

Opponent:
FAGOR, S.Coop

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step - (yes, after amendment)

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Case Number: T 0107/12 - 3.5.02

D E C I S I O N
of Technical Board of Appeal 3.5.02
of 22 November 2016

Appellant: (Patent Proprietor)	Unitron Frankrijklaan 27 8970 Poperinge (BE)
Representative:	Plas, Axel Ivo Michel IP HILLS NV Hubert Frère-Orbanlaan 329 9000 Gent (BE)
Respondent: (Opponent)	FAGOR, S.Coop Barrio San Andrés, s/n 20500 MONDRAGON (Guipuzcoa) (ES)
Representative:	Igartua, Ismael Fagor, S.Coop. Industrial Property Department San Andrés Auzoa, z/g; Apdo. 213 20500 Arrasate-Mondragon (ES)
Decision under appeal:	**Decision of the Opposition Division of the European Patent Office posted on 17 November 2011 revoking European patent No. 1794883 pursuant to Article 101(3)(b) EPC.**

Composition of the Board:

Chairman	R. Lord
Members:	M. Léouffre
	W. Ungler

Summary of Facts and Submissions

I. The proprietor appealed against the decision of the opposition division, dispatched on 17 November 2011, to revoke the European patent No. 1 794 883. The appeal was received on 17 January 2012, and the statement setting out the grounds of appeal was received on 19 March 2012.

II. The following documents cited by the opponent are relevant for the present decision:

D1: GB 2 272 341 A,
D2: US 5 337 338 A,
D5: GB 2 187 906 A,
D6: US 5 872 603 A,
D9: US 6 172 633 B1, and
D10: D.DeLauter, "A 256 Channel Control System Using FPGAs and a PLD", April 1996, Actel Corporation.

III. At the oral proceedings which took place before the board on 22 November 2016, the final request of the appellant (patent proprietor) was that the decision under appeal be set aside and the patent be maintained in amended form on the basis of the claims of the new main request filed during the oral proceedings.

The respondent (opponent) requested that the appeal be dismissed.

IV. Claim 1 of the now sole request reads as follows:

"An electronic filter device for the reception of TV-signals, comprising RF-circuitry having a plurality of frequency determining elements to filter a plurality of desired TV channels from an incoming signal, each

frequency determining element being settable by means of an analog setting voltage, a memory (2) storing digital values representative of the analog setting voltages and conversion circuitry (11-14) for converting the digital values into the analog setting voltages, characterised in that the conversion circuitry comprises:

a first fully digital part (11-13) integrated into a single chip, comprising an N-bit counter (11), a register (12) comprising at least MxN bits and M comparators (13) which are at least N-bit wide, for generating a digitally modulated signal for each digital value, the digitally modulated signal having a modulated characteristic representative of the digital value, the modulated characteristic being a duty cycle which is linked to the stored digital value and thus the voltage to be generated;

and a second part (14) for converting each of the digitally modulated signals into the analog setting voltages, the second part of the conversion circuitry comprising an integrator bank (14) with M integrators, one for each digitally modulated signal, the integrators being implemented in the form of RC-networks provided for generating the desired analog voltages from the digitally modulated signals, and an output bank (17) where the M analog setting voltages are presented, such that all analog setting voltages can be generated simultaneously."

Claims 2 to 5 are dependent on claim 1.

V. The appellant essentially argued as follows:

The invention aimed at filtering a plurality of TV-channels from an incoming signal.

The now sole request was filed in reaction to the objections of the board and should be seen as an attempt to address the objections of lack of support and clarity raised by the board in its annex to the summons and during the oral proceedings. It was based on the fifth auxiliary request filed with the grounds of appeal. It did not change the subject-matter for which protection was sought and comprised subject-matter which had been searched. Following the objection of the respondent that the last feature of claim 1 was originally disclosed in page 14 of the published application only in combination with the particular embodiments of figures 2 and 3, the essential features of the embodiment of figure 2 were introduced into claim 1. The features originated from page 8, lines 13 to 23. The other added feature: "the modulated characteristic being a duty cycle which is linked to the stored digital value and thus the voltage to be generated" originated from page 9, lines 20 to 22. Claim 1 was therefore clear and did not infringe Article 123(2) EPC. The request should therefore be admitted into the proceedings.

The closest state of the art was represented by D1 which was mentioned in the original description on page 1. Starting from D1 a person skilled in the art could have identified three different problems affecting the circuit disclosed therein, namely:

- the digital-to-analog converters (DACs) were expensive even if only four DACs were used;
- the refreshing algorithm used therein introduced complexity and ripples;
- the circuit was sequential and therefore slow, in particular during calibration.

A person skilled in the art trying to improve the circuit of D1 would not have applied the teaching of D5

which suggested to use one DAC per digital value because D5 did not aim at filtering a plurality of TV-channels and because DACs were expensive. A combination of D1 and D5 could have resulted only from hindsight.
D9 suggested that the use of digital-to-analog converters based on PWM technology could be a cheaper option, but that PWM-based DACs were to be used only when speed and precision were not an issue, as recited in D9, column 1, lines 15 to 20. Therefore D9 taught away from the invention.
At most, a person skilled in the art would have replaced the four DACs of D1 with PWM-based converters. The problems resulting from the use of the refreshing algorithm, like speed and ripples, would however not have been solved.
D2 disclosed that PWM-based converters were well known. No problem was mentioned in D2. Furthermore D2, column 1, lines 52 to 55 taught that PWM-based converters were slow. Thus, a person skilled in the art would not have combined D1 and D2.
D6 also taught away from the invention. D6 suggested not to use a plurality of PWM circuits but rather conventional digital-to-analog converters which were controlled in time-division manner (see first paragraph of the summary of invention of D6).
In D10, page 6-12, right-hand column line 3 and page 6-13, left-hand column, lines 18 to 20, the speed was also indicated as a potential problem.
The problem of speed and time, in particular the time for calibration, was not recognised in any of the prior art cited by the respondent. Hence a person skilled in the art, aware that the use of PWM-based digital-to-analog converters might be a cheaper option, would have at most replaced the conventional DACs of D1 by PWM-DACs. He would not have changed the whole circuit of D1 to integrate on a single chip a number of comparators

corresponding to the number of digital values used for filtering the plurality of TV-channels in order to generate simultaneously a corresponding number of analog setting voltages.

VI. The respondent argued essentially as follows:

Claim 1 of the sole request infringed Article 123(2) EPC. The feature "such that all analog setting voltages can be generated simultaneously" was based on page 14, lines 5 and 6. This feature was however disclosed there in combination with the devices of figures 2 and 3. Not all of the features of figure 2 recited in page 8, lines 13 to 23 had been incorporated into claim 1. The other features recited in the remaining part of page 8, i.e. lines 3 to 13, such as the microcontroller 1, the PC and user interface, had not been incorporated into claim 1, contrary to the guidelines. The requirements following from Article 123(2) EPC were therefore not met. These features might not have been essential, but essentiality was not a criterion for assessing the compliance with Article 123(2) EPC.

Furthermore, following Article 12(2) of the RPBA the request should not be admitted into the proceedings, since a complete case should have been filed with the statement of grounds of appeal. The appellant filed 8 auxiliary requests with the grounds of appeal followed by 6 new auxiliary requests filed with the letter of 12 October 2016. The new request constituted an abuse of procedure and was detrimental to procedural economy.

The subject-matter of claim 1 of the now sole request was also obvious.
Document D1, which represented the closest prior art, referred to D5 in which one DAC was used per digital

value. In D1, it was acknowledged that DACs were expensive. Therefore a new circuit was designed involving only four DAcs and a selector to store the sequentially generated set of four analog setting voltages in an analog memory 8 (see figure 1 of D1). Each of documents D2, D6, D9 and D10 revealed that it was known that PWM-based digital to analog converters constituted a cheap option to design digital analog converters (see in particular D9, column 1, lines 11 to 13 and D2, column 3 line 18). Indeed this formed part of the common general knowledge in the technical field. Hence a person skilled in the art, aware of this option, would have immediately recognised that not only the digital-to-analog converters 5 of D1 could be replaced by PWM circuits, but that it would be possible to revert to a solution wherein each set of analog voltages could be generated by its own set of PWM-DACs, whereby the whole selector 7 and refreshing algorithm of D1 could be dispensed with. The person skilled in the art would have therefore used one comparator and one integrator per digital value to be converted and would have arrived thereby at a circuit as claimed, bearing in mind that integrating comparators and integrators on a single chip was standard practice and could not be viewed as involving an inventive step. Hence the claimed invention was obvious in the light of the combination of D1 with either D2, D6, D9 or D10, or with common general knowledge.

Reasons for the Decision

1. The appeal is admissible.

2. Admissibility and Article 123(2) EPC

2.1 The new request was filed in reaction to the objection of lack of clarity raised by the board, in particular the objection that the features "An electronic filter device for the reception of TV-signals, comprising RF-circuitry having a plurality of frequency determining elements to filter a plurality of desired TV channels from an incoming signal" even in combination with the added feature f) "such that all analog setting voltages can be generated simultaneously" were not sufficient to define the invention.
Hence the board concludes that this request, which now comprises the means to simultaneously generate the setting voltages (see features c) to e) below), represents a valid attempt to remedy to the objections raised. The board therefore exercised it discretion under Article 13(1) and (3) RPBA to admit it into the proceedings.

2.2 Claim 1 is based on claim 1 as granted wherein:
(a) the device comprises "RF circuitry" having a plurality of frequency determining elements,
(b) "to filter a plurality of desired TV channels from an incoming signal",
(c) the first part of the conversion circuitry is "a first fully digital part (11-13) integrated into a single chip, comprising an N-bit counter (11), a register (12) comprising at least MxN bits and M comparators (13) which are at least N-bit wide", for generating a digitally modulated signal having

(d) a "modulated characteristic being a duty cycle which is linked to the stored digital value and thus the voltage to be generated", and
(e) "the second part of the conversion circuitry comprising(es) an integrator bank (14) with M integrators, one for each digitally modulated signal, the integrators being implemented in the form of RC-networks provided for generating the desired analog voltages from the digitally modulated signals, and an output bank (17) where the M analog setting voltages are presented",
(f) "such that all analog setting voltages can be generated simultaneously."

Feature a) is based on page 8, lines 20 to 23 of the description of the published application;
Feature b) is implicit from the description of the embodiments in the context of the cited problem;
Feature c) is based on page 4, line 14 and page 8, lines 15 and 16;
Feature d) is based on page 9, lines 20 to 22;
Feature e) is based on page 8, lines 16 to 20; and
Feature f) originates from the sentence: "With the figures 2 and 3, the speed can be increased as all analog voltages can be generated simultaneously" at page 14, lines 5 and 6.
Since all the features from figure 2 which are relevant for the definition of the invention have been incorporated in features c) and e) of the claim 1, Feature f) also does not contravene the requirements of Article 123(2) EPC.

The respondent referred to the examination guidelines, and contended that all the features relating to figure 2 which are mentioned at page 8 of the original description should have been introduced into the claim.

The board assumes that the Guidelines referred to are the Guidelines H-V, 3.2.1 which recite:
"When a feature is taken from a particular embodiment and added to the claim, it has to be established that:
- the feature is not related or inextricably linked to the other features of that embodiment and
- the overall disclosure justifies the generalising isolation of the feature and its introduction into the claim."

The board notes also that this provision is based on established case law of the boards of appeal.
In the present case the features relating to figure 2, which are not already recited in the claim, are listed at page 8, lines 6 to 13 of the original description as follows: "a microcontroller 1, a non-volatile memory 2 for storing all factory data and all settings made in the field by the installer, a PC-interface 3, for instance for firmware upgrades or changing the settings of the device, a user-interface logic 4 with user-interface input devices 5 and user-interface output devices 6, where items 4 through 6 are used for example for changing the settings, for showing an automatic equalization function, and any other possible functions, and an RF detection circuit 7 to detect the RF-level needed for automatic equalization function". The devices mentioned there are implicit in any micro-controlled apparatus, and the claimed conversion circuitry may be operated essentially independently of the above devices. The conversion circuitry according to the invention had even been designed to reduce load on the microcontroller, which now transfers the digital values from the non-volatile memory 2 to the register 12 without having to refresh these values. Hence the two criteria mentioned in the guidelines, which are

based on established case law of the boards of appeal, are satisfied.
The board thus concludes that the claim meets the requirements following from Article 123(2) EPC.

3. Article 54 EPC
Novelty of the claimed subject-matter was not contested.

4. Article 56 EPC

4.1 The parties agreed that D1 represents the closest prior art.
D1 discloses an electronic filter device for the reception of TV-signals, comprising RF-circuitry having a plurality of frequency determining elements to filter a plurality of desired TV channels from an incoming signal, each frequency determining element being settable by means of an analog setting voltage, a memory 3 for storing digital values representative of the analog setting voltages V_{s1} to V_{s4} and conversion circuitry 5, for converting the digital values into the analog setting voltages V_{s1} to V_{s32} (see figures 1 to 3 and page 5, line 10 to page 6, line 5).
The conversion circuitry of D1 comprises digital-to-analog converters and therefore necessarily a first fully digital part and a second part for converting each of the digitally modulated signals into the analog setting voltages.

4.2 The subject-matter of claim 1 differs from D1 by the features c) to f) mentioned in section 2.2 above.

Features c) and d) define a circuit for converting M digital values, which are at least N-bit wide, into M analog signals, each analog signal having a duty cycle

representing one of the M input digital values, and feature e) defines a circuit integrating each of the said analog signals to produce M analog values, each representing one of the M digital values. Thus, features c) to e) describe together a circuit comprising M digital-to-analog converters based on the well known pulse width modulation technology. DACs (digital-to-analog converters) based on pulse width modulation technology are indeed known to the person skilled in the art, and examples of PWM-based DACs are shown in each of documents D2, D6, D9 or D10. The appellant did not contest that PWM-based DACs were known at the date of filing.
As the respondent remarked, documents D2 and D9 give a clear indication that PWM-based DACs are cheaper than other more conventional DACs, and the board could agree that a person skilled in the art could have been inclined to make use of that technology when implementing the circuit of D1.

The person skilled in the art would have thereby immediately replaced the DACs 5 in D1 by four PWM-based DACs without exercising any inventive skill. He would have thus arrived at a circuit where the analog setting voltages would be available simultaneously for filtering a plurality of TV channels. Nevertheless he would not have achieved a circuit wherein all the M digital values used for filtering a plurality of TV-channels are converted simultaneously as recited in feature f). The setting voltages would instead have been sequentially generated using PWM-based digital-to-analog converters in place of the four DACs 5 of D1.

According to the appellant, the advantage of generating the M values simultaneously lies in the time saved for calibration of the non-volatile memory at the

production stage, as recited at page 14, lines 6 to 8 of the published application.

None of the available prior art documents addressed the problem of the calibration time. Hence the board concludes that the subject-matter of claim 1 is not obvious in the light of D1 in combination with any of documents D2, D6, D9 or D10, or with common general knowledge.

4.3 The respondent argued that, starting from D1, a person skilled in the art, aware of the fact that PWM-based digital-to-analog converters are cheaper than other more conventional DACs, would have abandoned the sequential production of the setting voltages as shown in D1 to come back to a circuit wherein each digital value is converted with its own DAC as shown in D5. The board is not convinced by this argument, since none of the available prior art documents recognises the problem of ripple resulting from the use of the selector 7 of D1, or the problem of calibration time, which results from the sequential production of the converted data, or the original problem mentioned in the description which relates to the load on the microcontroller caused by the refresh algorithm. Without identifying any of these problems a person skilled in the art would not have had any incentive to apply even a parallel configuration of PWM-based converters as shown in D10 (figures 1 and 2) to the system of D1. He would have simply implemented in a straightforward manner the four DACs 5 of D1 with PWM-based DACs. Therefore the board considers that the respondent's argument based on a combination of D1 with D5 and any of D2, D6, D9 or D10, or with common general knowledge, attempting to establish that a person skilled in the art would have reverted to a circuit for

filtering a plurality of TV-channels in which the number of sets of PWM-based DACs corresponds to the plurality of TV-channels, is based on hindsight.

5. Given these conclusions concerning claim 1, and noting that no further objections have been raised concerning this set of claims, the board concludes that they are suitable to form the basis of a patent maintained in amended form. Nonetheless, the board notes also that considerable amendments to the description would be necessary to adapt it to these amended claims, and therefore considers it to be appropriate to remit the case to the department of first instance for this to be carried out.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to maintain the patent on the basis of claims 1 to 5 of the main request filed during the oral proceedings of 22 November 2016 and a description to be adapted.

The Registrar: The Chairman:

U. Bultmann R. Lord

Decision electronically authenticated