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Datasheet for the decision of 25 July 2016

Case Number: T 2347/11 - 3.5.06

Application Number: 05026720.2

Publication Number: 1640847

IPC: G06F13/42

Language of the proceedings: EN

Title of invention:
Dynamic random access memory (DRAM) semiconductor device

Patent Proprietor:
Rambus Inc.

Former Opponent:
SK hynix Deutschland GmbH
MICRON EUROPE Ltd

Headword:
DRAM/RAMBUS 1

Relevant legal provisions:
EPC Art. 101
EPC 1973 Art. 100(c)

Keyword:
Grounds for opposition - extension of subject-matter (yes)

Decisions cited:
T 0331/87, G 0001/06

Catchword:

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Case Number: T 2347/11 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 25 July 2016

Appellant: (Patent Proprietor)	Rambus Inc. 1050 Enterprise Way, Suite 700 Sunnyvale, CA 94089 (US)
Representative:	Eisenführ Speiser Patentanwälte Rechtsanwälte PartGmbB Johannes-Brahms-Platz 1 20355 Hamburg (DE)
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Representative:	Tunstall, Christopher Stephen Carpmaels & Ransford LLP One Southampton Row London WC1B 5HA (GB)
Decision under appeal:	**Decision of the Opposition Division of the European Patent Office posted on 28 October 2011 revoking European patent No. 1640847 pursuant to Article 101(3)(b) EPC.**

Composition of the Board:

Chairman	W. Sekretaruk
Members:	A. Teale
	M. Müller

Summary of Facts and Submissions

I. This is an appeal by the patent proprietor, the sole appellant in these proceedings, against the decision by the opposition division, dispatched with reasons on 28 October 2011, to revoke European patent No. 1 640 847.

II. The patent derives from a second generation divisional application from a grandparent application which has been referred to in these proceedings as the "PCT application". More specifically, the present patent derives from European patent application No. 05 026 720.2, a divisional application of European patent application No. 00 100 018.1, which was itself a divisional application of European patent application No. 91 908 374.1, filed as International patent application No. PCT/US91/02590, the PCT application, which was published as WO 91/16680 A1 (referred to as P31 in the decision).

III. Claims 103 and 104 of the PCT application read as follows (emphasis by the board):

"103. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, **and has substantially fewer bus lines than the number of bits in a single address**, said semiconductor device comprising connection means adapted to connect said semiconductor device to said bus, and at least one

modifiable access-time register accessible to said bus through said connection means, whereby data may be transmitted to said register via said bus which establishes a predetermined amount of time that said semiconductor device thereafter must wait before using said bus in response to a request."

"104. The semiconductor device of claim 103 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus."

IV. Two oppositions were received against the granted patent. The opposition by opponent 1 (later respondent opponent 1) was based on the grounds of opposition foreseen in Article 100(a) (inventive step) and (c) (extension beyond the content of the earlier application as filed) EPC 1973. The opposition by opponent 2 (later respondent opponent 2) was based on the grounds of opposition foreseen in Article 100(a) (novelty, inventive step), (b) and (c) EPC 1973.

V. The reasons for the appealed decision stated *inter alia* that the patent according to the main and auxiliary requests I to IV extended beyond the content of the PCT application as filed, Article 100(c) EPC.

VI. A notice of appeal was received from the proprietor on 9 November 2011, requesting that the decision be set aside, that the oppositions be rejected and that the patent be maintained as granted (main request) or in amended form according to one of the auxiliary requests forming the basis of the decision. An auxiliary request was also made for oral proceedings. The appeal fee was paid on the same day.

VII. With a statement of grounds of appeal, received on 1 March 2012, the appellant proprietor refiled auxiliary requests I to IV upon which (with the exception of auxiliary request IIIa, filed in the oral proceedings) the appealed decision was based and requested that the oppositions be rejected and the decision set aside.

VIII. Reference is made to an interlocutory decision (also bearing the case number T 2347/11) relating to the present case dated 16 October 2012 by this board in a different composition. The decision was limited to the question of whether the appeal proceedings had been terminated by the apparent withdrawal of the application by the proprietor and did not go into the substantive matters of the case. The order of the decision stated *inter alia* that "The request for issuing a declaration that 'the appeal has been withdrawn'" was rejected.

IX. On 14 February 2013 a response to the appeal was received from respondent opponent 2, requesting that all of the appellant's requests be dismissed under Article 100(c) EPC and that the patent be revoked. An auxiliary request was also made for oral proceedings.

X. On 15 February 2013 a response to the appeal was received from respondent opponent 1, requesting that the appeal be dismissed and that the patent be revoked in its entirety, both as granted and as amended according to the auxiliary requests. An auxiliary request was also made for oral proceedings. A further auxiliary request was made to refer several questions to the Enlarged Board of Appeal under Article 112 EPC. As a further auxiliary request, it was requested that,

if the appealed decision were not confirmed regarding extension (Articles 100(c) and 76(1) EPC 1973) and/or "res judicata" or procedural abuse, that the case be remitted to the first instance for further prosecution on the basis of the remaining grounds for opposition that had been raised.

XI. In a letter received on 3 July 2013 respondent opponent 1 withdrew its opposition.

XII. In a letter received on 4 February 2014 respondent opponent 2 withdrew its opposition.

XIII. In a letter received on 8 March 2016 the appellant proprietor withdrew its request for oral proceedings and stated that "The patent proprietor does not intend to amend its case any further and rather requests a decision in accordance with the present status of the file."

XIV. Claim 1 according to the main request (the patent as granted) reads as follows:

"A Dynamic Random Access Memory (DRAM) semiconductor device having at least one memory array which includes a plurality of memory cells arranged in rows and columns, the DRAM comprising: connection means adapted to connect the DRAM to an external bus which is a part of a semiconductor bus architecture, the semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, the

connection means being adapted to receive multiplexed addresses; clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54); a programmable access-time register for storing a value which is representative of a first number of clock cycles of the external clock signal (53, 54) to transpire after which the DRAM responds to a write request received synchronously with respect to the external clock signal, the programmable access-time register being accessible to the external bus through the connection means, wherein to set the value in the programmable access-time register data is transmitted to the programmable access-time register over the external bus; and a plurality of input receivers (71, 72) to receive write data from the external bus in response to the write request, wherein the input receivers input the write data from the external bus after the first number of clock cycles transpire so that the write request and the corresponding receipt of write data are separated by the first number of clock cycles as selected by the value stored in the programmable access-time register."

XV. Claim 1 according to the first auxiliary request reads as follows (additions with respect to the main request being indicated in **bold**):

"A Dynamic Random Access Memory (DRAM) semiconductor device having at least one memory array which includes a plurality of memory cells arranged in rows and columns, the DRAM comprising: connection means adapted to connect the DRAM to an external bus which is a part of a semiconductor bus architecture, the semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus

lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, **and has fewer bus lines than the number of bits in a single address**, the connection means being adapted to receive multiplexed addresses; clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54); a programmable access-time register for storing a value which is representative of a first number of clock cycles of the external clock signal (53, 54) to transpire after which the DRAM responds to a write request received synchronously with respect to the external clock signal, the programmable access-time register being accessible to the external bus through the connection means, wherein to set the value in the programmable access-time register data is transmitted to the programmable access-time register over the external bus; and a plurality of input receivers (71, 72) to receive write data from the external bus in response to the write request, wherein the input receivers input the write data from the external bus after the first number of clock cycles transpire so that the write request and the corresponding receipt of write data are separated by the first number of clock cycles as selected by the value stored in the programmable access-time register."

XVI. Claim 1 according to the second auxiliary request reads as follows (additions with respect to the first auxiliary request being indicated in **bold**):

"A Dynamic Random Access Memory (DRAM) semiconductor device having at least one memory array which includes a plurality of memory cells arranged in rows and columns, the DRAM comprising: connection means adapted

to connect the DRAM to an external bus which is a part of a semiconductor bus architecture, the semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, and has **substantially** fewer bus lines than the number of bits in a single address, the connection means being adapted to receive multiplexed addresses; clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54); a programmable access-time register for storing a value which is representative of a first number of clock cycles of the external clock signal (53, 54) to transpire after which the DRAM responds to a write request received synchronously with respect to the external clock signal, the programmable access-time register being accessible to the external bus through the connection means, wherein to set the value in the programmable access-time register data is transmitted to the programmable access-time register over the external bus; and a plurality of input receivers (71, 72) to receive write data from the external bus in response to the write request, wherein the input receivers input the write data from the external bus after the first number of clock cycles transpire so that the write request and the corresponding receipt of write data are separated by the first number of clock cycles as selected by the value stored in the programmable access-time register.

XVII. Claim 1 according to the third auxiliary request reads as follows (additions with respect to the second auxiliary request being indicated in **bold**):

"A Dynamic Random Access Memory (DRAM) semiconductor device having at least one memory array which includes a plurality of memory cells arranged in rows and columns, the DRAM comprising: connection means adapted to connect the DRAM to an external bus which is a part of a semiconductor bus architecture, the semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, and has substantially fewer bus lines than the number of bits in a single address, the connection means being adapted to receive multiplexed addresses; **clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54) having a clock rate equal to a bus cycle data rate divided by two**; a programmable access-time register for storing a value which is representative of a first number of clock cycles of the external clock signal (53, 54) to transpire after which the DRAM responds to a write request received synchronously with respect to the external clock signal, the programmable access-time register being accessible to the external bus through the connection means, wherein to set the value in the programmable access-time register data is transmitted to the programmable access-time register over the external bus; and a plurality of input receivers (71, 72) to receive write data from the external bus in response to the write request, **wherein the input receivers input the write data from the external bus at the bus cycle data rate** after the first number of clock cycles transpire so that the write request and the

corresponding receipt of write data are separated by the first number of clock cycles as selected by the value stored in the programmable access-time register, **wherein the value stored in the programmable access-time register is further representative of a second number of clock cycles to transpire after which the DRAM responds to a read request received synchronously with respect to the external clock signal, wherein the DRAM outputs read data onto the bus at the bus cycle data rate in response to the read request after the second number of clock cycles and synchronously with respect to the external clock signal (53, 54), so that the read request and the corresponding response are separated by the second number of clock cycles as selected by the value stored in the programmable access-time register.**"

XVIII. Claim 1 according to the fourth auxiliary request reads as follows (additions with respect to the third auxiliary request being indicated in **bold**):

"A Dynamic Random Access Memory (DRAM) semiconductor device having at least one memory array which includes a plurality of memory cells arranged in rows and columns, the DRAM comprising: connection means adapted to connect the DRAM to an external bus which is a part of a semiconductor bus architecture, the semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, and has substantially fewer bus lines than the number of bits in a single address, the connection means being

adapted to receive multiplexed addresses; clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54) having a clock rate equal to a bus cycle data rate divided by two; a programmable access-time register for storing a value which is representative of a first number of clock cycles of the external clock signal (53, 54) to transpire after which the DRAM responds to a write request received synchronously with respect to the external clock signal, the programmable access-time register being accessible to the external bus through the connection means, wherein to set the value in the programmable access-time register data is transmitted to the programmable access-time register over the external bus; and a plurality of input receivers (71, 72) to receive write data from the external bus in response to the write request, wherein the input receivers input the write data from the external bus at the bus cycle data rate after the first number of clock cycles transpire so that the write request and the corresponding receipt of write data are separated by the first number of clock cycles as selected by the value stored in the programmable access-time register, wherein the value stored in the programmable access-time register is further representative of a second number of clock cycles to transpire after which the DRAM responds to a read request received synchronously with respect to the external clock signal, wherein the DRAM outputs read data onto the bus at the bus cycle data rate in response to the read request after the second number of clock cycles and synchronously with respect to the external clock signal (53, 54), so that the read request and the corresponding response are separated by the second number of clock cycles as selected by the value stored in the programmable access-time register; and **a plurality of sense**

amplifiers used for sensing the read data from the memory array, wherein when precharge information received over the external bus indicates that a precharge operation should be performed, automatically precharging a portion of the memory array and the sense amplifiers as a part of execution of the read request."

Reasons for the Decision

1. The admissibility of the appeal

The appeal fulfills the admissibility criteria under the EPC and is consequently admissible.

2. The technical context of the invention

The present invention concerns a dynamic random access memory (DRAM) semiconductor device having at least one memory array which includes a plurality of memory cells arranged in rows and columns; see figure 1. Sense amplifiers are used to read data from the memory array. The device also contains connection means for connecting it to an external bus which is a part of a semiconductor bus architecture comprising a plurality of semiconductor devices connected in parallel to the external bus; see figure 2. The connection means include input receivers for receiving data from the external bus. The external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus. The device further contains a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal

to transpire after which the DRAM responds to a write request received synchronously with respect to the external clock signal.

3. The request to refer questions to the Enlarged Board of Appeal

Former respondent opponent 1 requested that, if the appeal was not dismissed and the patent as granted or as amended according to auxiliary requests I to IV was not revoked, that various questions be referred to the Enlarged Board of Appeal. Since respondent opponent 1 has withdrawn its opposition (see point XI above), it is no longer a party to these proceedings and its requests need no longer be considered. However, in view of the board's decision, respondent opponent 1's own conditions for a referral are not met. The board also sees no reason to refer questions to the Enlarged Board of Appeal of its own motion.

4. The ground of opposition under Article 100(c) EPC 1973

4.1 According to the appealed decision, the patent according to the main and auxiliary requests extended beyond the content of the PCT application as filed, Article 100(c) EPC 1973.

4.2 Since the filing date of the patent (16 April 1991) lies before the entry into force of EPC 2000 on 13 December 2007, Article 100(c) EPC 1973 is applicable to the present case. Moreover, since the patent had already been granted at the time of entry into force of EPC 2000, the decision to grant being dated 18 May 2007, Article 101 EPC also applies to the present case.

4.3 According to Article 101(2) EPC, if the opposition division is of the opinion that at least one ground for opposition prejudices maintenance of the European patent, it shall revoke the patent. This applies both to the patent as granted (main request) and to the amended patent (auxiliary requests). One of the grounds for opposition relied upon by the former respondent opponents is that set out in Article 100(c) EPC 1973, namely that the subject-matter of the European patent extends beyond the content of the earlier application as filed. In the present case the parties, the opposition division and the board all understand the expression "earlier application" as referring to the PCT application. This understanding is consistent with the analysis of a sequence of divisional applications set out in G 1/06 (OJ EPO 2008, 307); see headnote.

5. The appellant proprietor's main request

5.1 According to the reasons for the appealed decision (see point 5), the feature (referred to as "M2") that "[the bus] has substantially fewer bus lines than the number of bits in a single address", present in independent claim 103 of the PCT application, is not present in claim 1 of the main request. The proprietor argued that claim 1 of the main request set out, albeit in a different way, the subject-matter of dependent claim 104 in combination with independent claim 103 in the PCT application in stating that the device comprises "connection means adapted to connect the DRAM to an external bus" (feature "c" in the decision), "the connection means being adapted to receive multiplexed addresses" (feature "f" in the decision), summarized as "a bus with multiplexed addresses" below. In its decision the opposition division took the view that a bus having multiplexed addresses was more general than

a bus having substantially fewer bus lines than the number of bits in a single address. For example, a bus with 24 bit lines and 16 bits in a single address, the 16 address bits being sent over only 4 bits of the bus, would not fall within the definition "[the bus] has substantially fewer bus lines than the number of bits in a single address" but would fall within the definition of having "a bus with multiplexed addresses".

5.2 In the grounds of appeal the appellant proprietor argued *inter alia* (see pages 17 and 43 ff.) that claim 1 of the main request was based on claim 103 of the PCT application and, in the example given in the decision, the four bits of the bus used to send the address would themselves constitute a "bus", this "bus" having substantially fewer bus lines than the number of bits (sixteen in the example) in a single address, claim 103 not requiring that all the connections to the DRAM device be via the "bus". The appellant proprietor has also pointed out that claim 1 sets out a DRAM device, not DRAM with a bus. Not only the DRAM according to claim 103 of the PCT application but also the DRAM according to claim 1 of the main request was capable of use with the bus given in the example in the decision, the definition in claim 1 of the main request being narrower, not broader, than the definition in claim 103 of the PCT application. The appellant proprietor also argued that whatever features of the DRAM device had been removed from claim 1 with respect to claim 103 of the PCT application, the "three prong test" according to T 0331/87 showed that subject-matter had not been added.

5.3 Former respondent opponent 1 argued *inter alia* (see submission received on 15 February 2013, section C II,

i.e. pages 40 to 85, summarized on pages 84 and 85) that the expressions "capable of use" and "connection means adapted to connect ..." cause the features of the bus to limit those of the DRAM device. The expression in claim 1 of the main request "the connection means being adapted to receive multiplexed addresses" (AM) was broader than the expression "and has substantially fewer bus lines than the number of bits in a single address" (M2) in claim 103 of the PCT application. Also claim 104 in combination with 103 did not provide a basis for feature "AM". The relevance of T 0331/87 to the present case was questioned because claim 1 had been amended with respect to claim 103 of the PCT application in a manner that was more complex than simply deleting or replacing a feature. Moreover feature "M2" was present in all independent claims in the PCT application setting out the bus and thus must be regarded as essential in the disclosure. The description only disclosed a single bus according to the invention. Regarding the example set out in the decision, it was pointed out that all address, data and control information would be transmitted using the 24 bit lines of the external bus, as set out in feature "e" of claim 1: "wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus". Hence in the example all 24 bit lines constituted the "bus", not just four of them, as asserted by the appellant proprietor. Respondent opponent 1 conceded that it was clear from claims 103 and 104 of the PCT application that the claimed device could be connected to several differing busses; an exhaustive list of all bus lines was not set out in the claims. However claim

103 set out at least an adaption of the device to the specified bus.

5.4 Former respondent opponent 2 also argued *inter alia* that the expression in claim 1 of the main request "the connection means being adapted to receive multiplexed addresses" (the "narrow bus feature") was broader than the expression "and has substantially fewer bus lines than the number of bits in a single address" in claim 103 of the PCT application.

5.5 The disclosure in the PCT application

5.5.1 The bus

According to the summary of the invention in the PCT application, the bus "includes clock signals, power and multiplexed address, data and control signals"; see page 8, lines 1 to 2. The description then gives an example of the bus, which the board understands to be illustrated in figure 2 (see, in particular, lines BUSDATA[0]-[7], CLOCK1, CLOCK2, GND, V_{DD}): "In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide". The section entitled "Bus" also concerns eight multiplexed bus lines (BusData[0:7]) carrying address, data and control signals; see page 18, line 21, to page 19, line 21. The board understands this disclosure to mean that the address, data and control signals are all carried by the same multiplexed bus lines, albeit at different times. The bus has substantially fewer bus lines than the number of bits in a single address (see page 7, lines 16 to 17) because an address word is split into several parts (see figure 4) before being sent over the multiplexed bus lines and then

reassembled, a technique acknowledged as prior art in the description; see page 2, line 23, to page 3, line 3. In the light of this disclosure, the board does not accept the appellant proprietor's argument that the "bus" can be considered to be only those lines carrying parts of address words, since the bus is disclosed as not only comprising multiplexed address, data and control signals, but also clock signals and power lines, as illustrated in figure 2; see the lines CLOCK1, CLOCK2, GND and V_{DD}. The fact that the bus disclosed in the PCT application uses address multiplexing, a technique acknowledged as being conventional in the description, does not necessarily mean that the skilled person would have understood address multiplexing to be optional. Moreover the feature that the bus has substantially fewer bus lines than the number of bits in a single address is not understood as a synonym for a bus using address multiplexing, since the description makes clear that the bus is also used to carry data and control signals; see page 8, lines 1 to 2. Address multiplexing implies a limitation of the number of device address pins but not a limitation on the number of data and control pins. Hence a device having address multiplexing may connect to a bus having few multiplexed bus lines but an unspecified number of data and control lines, so that the entire bus to which it is adapted to connect need not have substantially fewer bus lines than the number of bits in a single address. Hence, as the opposition division put it, the feature of "address multiplexing" is broader than the feature that "the bus has substantially fewer bus lines than the number of bits in a single address".

5.5.2 The multiple-bus embodiments

Figure 3 illustrates three DRAM devices (15, 16, 17) having pins on one side, the pins being connected directly to the "primary" bus 18; see page 10, line 12. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20; see page 9, lines 19 to 22. Figure 9 shows an embodiment with a higher level of integration where several "subsystems", each comprising DRAM devices (15, 16, 17), a primary bus (18) and a transceiver (19), are all connected via their respective transceiver to a "transceiver bus" (65): see page 49, lines 8 to 12. The board finds it significant that, although multiple bus arrangements comprising a plurality of said subsystems are discussed, the connection to the DRAM devices themselves remains in every case the "primary bus".

5.5.3 The semiconductor device interface

Claim 1 of the patent and claim 103 of the PCT application refer to "connection means". The board understands these in the context of the "device interface" disclosed from page 53, line 4, to page 59, line 2, of the PCT application. The device interface comprises the electrical interface comprising input receivers, bus drivers and clock generation circuitry. The board understands from this that the features of the connection means reflect the features of the primary bus, in particular the functions of the various bus lines. In other words, contrary to the argument by the appellant proprietor, the features of the bus do imply a restriction of the features of the DRAM device to at least be adapted to the narrow bus mentioned in original claim 103. As disclosed in original claims (or "embodiments") 82 and 92, the connecting means consists

of pins for connection to the external bus and corresponding wires for connection with the internal bus logic. The adaptation of the semiconductor device for connection to the narrow bus does not limit the number of pins that the semiconductor device has, as there may be unused pins just as there may be unused bus lines. However, the number of pins carrying bus signals is determined by the internal bus logic. Thus the "narrow bus" feature in combination with the connecting means adapted to it implies that the claimed semiconductor device "has substantially fewer" pins carrying bus signals "than the number of bits in a single address".

5.6 The amendments to claim 1 of the main request

5.6.1 The board agrees with the parties that claim 103 of the PCT application forms the basis for claim 1 of the present main request, various features having been either added or deleted. In particular, the feature that the bus "has substantially fewer bus lines than the number of bits in a single address" (the "narrow bus" feature "M2") has been deleted, and *inter alia* the feature that the connection means are "adapted to receive multiplexed addresses" (the "multiplexed address" feature "MA") has been added.

5.6.2 The appellant proprietor has argued that claims 103 and 104 and the description of the PCT application provide a basis for both amendments. The board disagrees. All of the independent claims in the PCT application setting out a bus, including claim 103, contain the feature that the bus has "substantially fewer bus lines than the number of bits in a single address". This is consistent with the example given on page 8, lines 2 to 4, of memory addresses being up to 40 bits wide but the

bus having only twelve lines (see figure 2), namely clock lines CLOCK1 and CLOCK2, power lines V_{DD} and GND, and multiplexed address, data and control signals BUSDATA[0]-[7]. The appellant proprietor has argued that the two features "M2" and "MA" referred to above, have the same meaning. As stated above (see point 5.5.1), the board disagrees, finding the feature of "address multiplexing" to be broader than the feature that "the bus has substantially fewer bus lines than the number of bits in a single address". As stated above, address multiplexing implies a limitation of the number of device address pins but not a limitation on the number of data and control pins. Hence the replacement of the "narrow bus" feature by the "address multiplexing" feature causes claim 1 to cover bus configurations that were not directly and unambiguously derivable from the PCT application as originally filed.

5.6.3 Claim 104 of the PCT application, which sets out the device connecting substantially only to said bus and sending and receiving substantially all address, data and control information over said bus, restricts the features of the device rather than those of the bus itself. For this reason the board does not accept the appellant proprietor's argument that, in the light of claim 104, claim 103 can be understood as disclosing a more general bus having fewer lines. Hence the arguments based on claim 104 do not change the analysis, set out above, of claim 1.

5.6.4 Consequently the board finds that the subject-matter of claim 1 according to the main request extends beyond the content of the PCT application as filed. Hence Article 100(c) EPC 1973 prejudices maintenance of the patent as granted, Article 101(2) EPC.

6. The appellant proprietor's auxiliary requests I and II

6.1 Claim 1 according to all four auxiliary requests sets out the features of the bus defined in claim 103 of the PCT application including the feature (M2) that the bus has (substantially) "fewer bus lines than the number of bits in a single address". For this reason these requests overcome the objections raised above against the main request.

6.2 According to the reasons for the appealed decision (point 8.1), the fact that claim 1 of auxiliary request II sets out an access-time register for a "write request", but not for a read request, causes it to extend beyond the content of the PCT application as filed, which sets out in claim 103 a modifiable access-time register for "a request".

6.3 The appellant proprietor has not disputed this finding, no specific arguments for auxiliary request II being provided in the part of the statement of grounds of appeal relating to the auxiliary requests; see pages 131 to 133.

6.4 The board notes that this objection not only applies to auxiliary request II but also to auxiliary request I. The access time required by the DRAM to respond to a read or write request is stored in a programmable register, expressed as a number of clock cycles of the external clock signal; see page 21, lines 8 to 20, of the PCT application. The only original claims setting out the register and a request, namely claims 103 and 121, both use the general term "request" and are not limited to either reading or writing. According to page 21, lines 15 to 20, "The timing of data for reads and writes is preferably the same; the only difference is

which device drives the bus. For reads, the slave drives the bus and the master latches the values from the bus. For writes the master drives the bus and the selected slave latches the values from the bus". In view of this disclosure, the board finds that it would not be directly and unambiguously derivable for the skilled person that, instead of the access time for all requests, only the access time for write requests could be stored in an access-time register.

6.5 Consequently the patent amended according to auxiliary requests I and II relates to subject-matter extending beyond the content of the earlier application as filed. Hence Article 100(c) EPC 1973 prejudices maintenance of the patent in these forms, Article 101(2) EPC.

7. The appellant proprietor's auxiliary requests III and IV

7.1 Claim 1 overcomes the objection raised above against that of auxiliary requests I and II in referring to both read and write requests.

7.2 According to the reasons for the appealed decision (point 9.1), the amendment of claim 1 to set out a single value stored in the programmable access-time register being representative of both a first and a second number of clock cycles of the external clock signal to transpire after which the DRAM responds to a write and a read request, respectively, caused claim 1 to extend beyond the content of the PCT application as filed. The cited passage on page 21, lines 15 to 16, of the description stating that "The timing of data for reads and writes is preferably the same ..." disclosed the possibility of different read and write times, but did not disclose how this was implemented.

7.3 The appellant proprietor has argued that claim 103 of the PCT application, setting out a programmable access-time register containing data establishing a predetermined amount of time that the device must wait before using the bus in response to a request, and page 21, lines 15 to 16, provided a basis for the amendment.

7.4 The board is not persuaded by the appellant's argument because the storage of a single value in the access-time register to represent both read and write access times does, as the decision says, go beyond the disclosure in the PCT application that the read and write times are the same in a way which would not have been direct and unambiguous for the skilled person. Also the statement in claim 103 that data stored in the register establishes a predetermined amount of time that the device must wait before using the bus in response to a request does not directly and unambiguously disclose the storage of a single value in the access-time register to represent both read and write access times.

7.5 Consequently the patent amended according to auxiliary requests III and IV relates to subject-matter extending beyond the content of the earlier application as filed. Hence Article 100(c) EPC 1973 prejudices maintenance of the patent in these forms, Article 101(2) EPC.

8. Hence the board finds that none of the appellant proprietor's substantive requests is allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

B. Atienza Vivancos W. Sekretaruk

Decision electronically authenticated