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Datasheet for the decision of 10 July 2014

Case Number: T 1963/11 - 3.5.01

Application Number: 02799229.6

Publication Number: 1468367

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Language of the proceedings: EN

Title of invention:
MULTITHREADED PROCESSOR WITH EFFICIENT PROCESSING FOR CONVERGENCE DEVICE APPLICATIONS

Applicant:
Qualcomm Incorporated

Headword:
Multithreaded processor/QUALCOMM

Relevant legal provisions:
EPC 1973 Art. 56, 84
EPC Art. 123(2)

Keyword:
Inventive step - (no)
Claims - clarity (no)
Amendments - added subject-matter (yes)

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Case Number: T 1963/11 - 3.5.01

D E C I S I O N
of Technical Board of Appeal 3.5.01
of 10 July 2014

Appellant: (Applicant)	Qualcomm Incorporated 5775 Morehouse Drive San Diego, CA 92121-1714 (US)
Representative:	Williams, David John Page White & Farrer Bedford House John Street London WC1N 2BF (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 7 April 2011 refusing European patent application No. 02799229.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	S. Wibergh
Members:	P. Scriven
	D. Prietzel-Funk

Summary of Facts and Submissions

I. This appeal is against the decision of the Examining Division to refuse European patent application No. 02799229.6. The application was published as WO 03/054714 A1.

II. The decision of the Examining Division refers to the following documents:

D1: Choquette J et al: "High-performance RISC microprocessors", IEEE Micro, vol. 19, no. 4, July 1999, pages 48-55, IEEE, Los Alamitos, CA, US.

D2: Yadav N et al: "Parallel saturating fractional arithmetic units", Proceedings Great Lakes Symposium on VLSI, 4 March 1999, pages 214-217, IEEE.

D5: Schulte M et al: "Parallel saturating multioperand adders", CASES '00, November 17-19, 2000, San Jose, CA, US, ACM 2000.

III. The Examining Division refused the main request and the first auxiliary request on the ground of lack of inventive step (Article 56 EPC). The Examining Division considered that the invention according to claim 1 of the main request would have been obvious in view of the combination of D1 and D5, or that of D1 and D2. Concerning the first auxiliary request, the Examining Division argued that, although there might seem to be a multitude of differences between claim 1 and D1, these differences were nothing more than an aggregation of known or obvious implementation details in view of the combined teaching of D2 and D5.

IV. The appellant filed an appeal against the decision and requested that the decision under appeal be set aside and that a patent be granted on the basis of a main request, a first auxiliary request, or a second auxiliary request, all requests filed with the statement setting out the grounds of appeal. The main request as filed with the grounds of appeal was said to correspond to the claims as refused by the Examining Division. The appellant also requested oral proceedings as an auxiliary measure.

V. In a communication accompanying a summons to oral proceedings, the Board noted that the main request and the first auxiliary request, as filed with the grounds of appeal, were identical. The Board stated its assumption that this was a mistake, and that the main request should have been the same as the main request refused by the Division, as stated in the grounds of appeal. The Board also provided its preliminary opinion that neither the main request nor the first auxiliary request appeared to involve an inventive step, and that the second auxiliary request appeared to give rise to issues under Articles 84 and 123(2) EPC.

VI. The appellant informed the Board that it would not attend the scheduled oral proceedings and requested a decision "on the basis of the file as it stands". The appellant did not provide any further arguments in support of its case.

VII. Claim 1 of the main request before the Examining Division reads as follows:

"A multithreaded processor (102) comprising:

an instruction decoder (116) for decoding retrieved instructions to determine an instruction type for each of at least a subset of the retrieved instructions;

an integer unit (118, 150, 152, 154) coupled to the instruction decoder for processing integer type instructions received from the instruction decoder; and

a vector unit (160) coupled to the instruction decoder for processing vector type instructions received from the instruction decoder, the vector unit comprising a plurality of parallel branches, each branch of which includes an accumulator;

characterised in that the processor further comprises:

a reduction unit (164) associated with the vector unit and receiving parallel data elements processed in the vector unit, the reduction unit generating a serial output from the parallel data elements".

VIII. Claim 1 of the first auxiliary request filed with statement setting out the grounds of appeal reads:

"A multithreaded processor (102) comprising:

an instruction decoder (116) for decoding retrieved instructions to determine an instruction type for each of at least a subset of the retrieved instructions;

an integer unit (118, 150, 152, 154) coupled to the instruction decoder for processing integer type instructions received from the instruction decoder; and

a vector unit (160) coupled to the instruction decoder for processing vector type instructions received from

the instruction decoder, the vector unit comprising a plurality of parallel branches, each branch including:

a vector file (162) for storing vector data;

a first register coupled to the vector file (162) for storing vector data retrieved from the vector file;

a multiplier coupled to the first register and configured to perform parallel multiplication on the vector data;

a second register coupled to the multiplier and the first register for storing intermediate results;

one or more add units coupled to the second register configured to perform additional arithmetic operations;

an accumulator register coupled to the one or more add units and to the vector file (162);

a reduction unit (164) coupled to the accumulator register for receiving parallel data elements processed in the vector unit (160), the reduction unit configured to generating [sic] a serial output from the parallel data elements; and

a results register coupled to the reduction unit (164) for storing the result of the processed data elements".

IX. Claim 1 according to the second auxiliary request differs from the first auxiliary request in that the vector unit further comprises:

"a vector instruction queue (156) having an input coupled to an output of the instruction decoder;

a vector file (162) having an input coupled to an output of the vector instruction queue;

an offset unit (158) having an output coupled to an input of the vector file;

at least one arithmetic element having an input coupled to an output of the vector file".

X. The appellant's arguments can be summarized as follows:

The invention provided a solution to the problem of efficiently and accurately processing vector type instructions in parallel in a multithreaded processor without introducing additional hardware or logic.

Neither D5 nor D2 addressed multithreading and the associated design considerations. Therefore, the skilled person would not have considered the structures disclosed in D5 and D2 for inclusion in a multithreaded processor.

Furthermore, D5 failed to disclose a "vector unit" for processing vector type instructions, the vector unit comprising a plurality of parallel branches. The extent to which D5 discussed vectors was limited to applying the adder arrangement taught to perform saturation addition on vector elements.

D5 also failed to disclose a "reduction unit" for receiving parallel data elements.

Additionally, D5 did not disclose the arrangement of components in the parallel branches as defined in the first auxiliary request and the Examining Division had

failed to show why the skilled person would have arrived at this particular arrangement.

XI. Oral proceedings took place in the absence of the appellant. At the end of the oral proceedings, the Board announced its decision.

Reasons for the Decision

1. *The invention*

1.1 The invention concerns a multithreaded processor. The application explains "multithreaded processor" as a processor that supports the simultaneous execution of multiple instruction sequences, called "threads" (page 1, lines 20-21, of the published application).

1.2 The multithreaded processor according to the invention comprises an instruction decoder for decoding retrieved instructions, an integer unit for executing integer type instructions, and a vector unit for executing vector type instructions. The application does not define the difference between "integer type instructions" and "vector type instructions". In the Board's understanding, an integer instruction operates on single data elements (integers), whereas a vector instruction operates on arrays of data elements (vectors). For example, whereas an integer instruction "ADD" adds the integer operands stored in registers R1 and R2, the corresponding vector instruction adds the vector operands in vector registers V1 and V2, element by element.

1.3 The vector unit, according to the invention, comprises a plurality of parallel branches which process "data elements" in parallel. According to the description on page 3, lines 5 to 6, the vector unit is a single instruction multiple data (SIMD) processing unit. The Board understands this to mean that each of the plurality of branches simultaneously performs the same operation on a vector data element such that the vector unit as a whole operates on multiple data elements. The processor also comprises a reduction unit which receives the parallel data elements processed in the vector unit and generates a serial output. This output is substantially the same as that which would be produced if the values computed in parallel in the vector unit were instead computed serially (page 6, lines 3-7).

1.4 The branches of the vector unit include a number of components for performing the operations specified by the vector type instructions, e.g. a multiplier (MPY), an adder (ADD) and an accumulator (ACC), as shown in figure 1.

2. *Main request, inventive step (Articles 52(1) EPC and 56 EPC 1973)*

2.1 With the statement setting out the grounds of appeal, the appellant submitted a set of claims, labelled "MAIN REQUEST", which were verbally identical to the claims according to the "FIRST AUXILIARY REQUEST" submitted at the same time. Since the statement setting out the grounds of appeal stated in this respect that "the main request corresponds to the claims as refused by the Examining Division", the Board understands the latter as expressing the intention of the appellant to further

pursue the refused claims. This view has been communicated to the appellant in the annex accompanying the summons to oral proceedings, and the appellant has not objected.

2.2 The Examining Division chose the processor disclosed in D1 as the starting point for the invention as defined in claim 1 and identified the following differences:

i) the vector unit comprises a plurality of parallel branches,

ii) each branch includes an accumulator; and

iii) the processor comprises a reduction unit receiving parallel data elements processed in the vector unit.

The appellant has not contested this and the Board sees no reason to question the Examining Division's assessment of D1.

2.3 D1 does not disclose the details of the vector unit. Thus, starting from D1, the Board agrees with the Examining Division that the differences (i) to (iii) solve the problem of providing a suitable structure for the vector unit. The reduction unit in claim 1, which receives the parallel data elements as input, and produces a serial output, is considered to be part of this structure.

2.4 The skilled person looking to provide a suitable structure for a vector unit would consider D2. This document is mentioned in the published application, on page 6, lines 9-12, as providing an implementation of the reduction unit and other portions of the vector unit according to the invention. D2 discloses a vector

unit having parallel branches (the dual-MAC Unit in figure 6), and a reduction unit for generating a serial output from the parallel data elements, the output being the same as the result of the operations performed serially (page 214, section "1. Introduction", third paragraph; pages 216 to 217, section "5. Saturating Dual MAC Unit"). Including this structure as the vector unit in the processor of D1 would result in the subject-matter of claim 1. The question is thus if the skilled person would have been led to combine the two documents.

2.5 The appellant argued that the invention provided a solution to the problem of efficiently and accurately processing vector type instructions in parallel in a multithreaded processor without introducing additional hardware or logic. In this context, the appellant mentioned the problem of stalling, which was said to occur when an instruction required an operand that was the result of a process that had not yet finished. In the prior art, stalling was often avoided by additional hardware or logic. Inaccurate results due to fixed point arithmetic, or to one thread overwriting data from another thread, were, according to the appellant, also a problem that occurred in the processing of vector instructions. The appellant argued that the invention provided a solution to the problems of stalling and inaccuracy by providing a vector unit with parallel branches, each branch processing the vector data elements independently of the concerns with stalling or inaccuracies. Since D2 did not address the problems associated with multithreading, the skilled person would not have included the structure disclosed in D2 in a multithreaded processor.

2.6 However, the Board does not see any consideration particular to multithreading addressed by the features of claim 1. The claim merely mentions that the processor is "multithreaded". In particular, there are no aspects of multithreading in the parallel processing of vector data elements in the vector unit as defined in claim 1. The vector unit receives an instruction from a given thread and executes it, independently of any multithreading issues. The problem of stalling is mentioned in the published description on page 6, lines 15-21, as arising in the context of pipelined instruction processing, but that is not part of the invention as claimed. Furthermore, the problem of inaccuracies has already been solved in D2 (by the saturating vector unit including a reduction unit; this is also implicit from the application itself which refers to D2 for the implementation of the vector unit). A reason for the skilled person to include the vector unit known from D2 was simply that this circuit was known to be useful (it is suitable for performing speech coding according to the GSM standard, as stated in the first paragraph of this document). Thus the subject-matter of claim 1 according to the main request does not involve an inventive step.

3. First auxiliary request - inventive step (Articles 52(1) EPC and 56 EPC 1973)

3.1 Claim 1 of the first auxiliary request, which has not been amended on appeal, differs from the main request in that it specifies a number of components included in each of the plurality of branches, namely:

a vector file for storing vector data;

a first register coupled to the vector file for storing vector data retrieved from the vector file;

a multiplier coupled to the first register and configured to perform parallel multiplication on the vector data;

a second register coupled to the multiplier and the first register for storing intermediate results;

one or more add units coupled to the second register configured to perform additional arithmetic operations;

an accumulator register coupled to the one or more add units and to the vector file;

a reduction unit coupled to the accumulator register for receiving parallel data elements processed in the vector unit, the reduction unit configured to generating [sic] a serial output from the parallel data elements;

and a result register coupled to the reduction unit for storing the result of the processed data elements.

3.2 The Examining Division considered that only the vector file and the various registers were not disclosed in D1 or D2; these were however nothing else but obvious details of implementation. The Board agrees, especially as the present application does not mention any particular problems solved by these features, and even refers to D2 for implementation details (cf. point 2.4 above).

3.3 For these reasons, the Board confirms the Examining Division's conclusion in the decision under appeal that

claim 1 according to the first auxiliary request does not involve an inventive step.

4. *Second auxiliary request - Articles 84 and 123(2) EPC*

4.1 The Board raised a number of issues concerning clarity (Article 84 EPC) and added matter (Article 123(2) EPC) in the communication accompanying the summons to oral proceedings. The appellant has not commented on this. The Board confirms the objections and concludes that the second auxiliary request is not allowable for the following reasons.

4.2 Claim 1 defines "vector file (162)" twice: as one file comprised in the vector unit and having an input coupled to an output of the vector instruction queue; and as a plurality of files, one in each branch, for storing vector data. Since the two definitions do not agree, the Board considers that claim 1 is not clear (Article 84 EPC).

4.3 Claim 1 defines an "offset unit (158) having an output coupled to an input of the vector file". In the Board's view, this definition is not sufficient to allow the reader to understand the function of this feature. In particular, it is not clear what is offset by this unit or how this would be done (Article 84 EPC).

4.4 The "arithmetic element having an input coupled to an output of the vector file" in claim 1 is in addition to the arithmetic units defined for the branches. The Board does not see a basis for such an additional unit in the application as filed. For this reason, claim 1 contravenes Article 123(2) EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

T. Buschek S. Wibergh

Decision electronically authenticated