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**Datasheet for the decision  
of 12 October 2017**

**Case Number:** T 1642/11 - 3.5.01

**Application Number:** 01901833.2

**Publication Number:** 1402329

**IPC:** G06F13/40

**Language of the proceedings:** EN

**Title of invention:**

LOW LATENCY MULTI-LEVEL COMMUNICATION INTERFACE

**Applicant:**

Rambus Inc.

**Headword:**

Bus driver / Rambus

**Relevant legal provisions:**

EPC Art. 56, 84, 123(2)

**Keyword:**

Inventive step - converting voltage mode driver to current mode  
(yes - no teaching in the prior art of how to do so)  
Clarity (yes - after amendment)  
Support by the description (yes - after amendment)  
Amendments - added subject-matter (no - after amendment)  
Length of oral proceedings



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Case Number: T 1642/11 - 3.5.01

**D E C I S I O N**  
**of Technical Board of Appeal 3.5.01**  
**of 12 October 2017**

**Appellant:** Rambus Inc.  
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**Representative:** Eisenführ Speiser  
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**Decision under appeal:** Decision of the examining division of the  
European Patent Office posted on 3 March 2011  
refusing European patent application No.  
01901833.2 pursuant to Article 97(2) EPC.

**Composition of the Board:**

**Chairman** P. Scriven  
**Members:** A. Wahrenberg  
I. Beckedorf

## **Summary of Facts and Submissions**

- I. The appeal is against the decision of the examining division to refuse the European patent application No. 01901833.2, published as WO 01/50228 A2, for lack of inventive step (Article 56 EPC) over D5 (US 5 793 816 A).
- II. In the statement setting out the grounds of appeal, the appellant requested that the decision of the examining division be set aside and that a patent be granted on the basis of the main request or auxiliary requests I to IV identified in the appealed decision.
- III. The Board arranged for oral proceedings to be held over two consecutive days. In the communication accompanying the summons to oral proceedings, the Board raised objections under Articles 84 and 123(2) EPC. The Board considered that, in view of the extensive problems of added subject-matter, lack of clarity, and lack of support by the description and drawings, no meaningful opinion could be given on inventive step in respect of the claims as they stood. However, the Board made some observations on the subject-matter disclosed in figure 30 of the published application, in view of D5 and D7 (US 5 254 883 A, cited by the Board).
- IV. With the reply, the appellant submitted five requests (auxiliary requests IA, IIA, IIIA, IVA and V) in addition to the five request already on file.
- V. Oral proceedings took place on 12 October 2017 as scheduled. The appellant filed nine further requests, which were considered by the Board. At the end, the appellant maintained only one request ("new request

12 October 2017 16:13h", Annex I), and withdrew all the other requests on file.

VI. Claim 1 of this request reads:

*A current mode output driver to drive on a multi-drop bus, an output symbol representing two bits including a most significant bit (MSB) and a least significant bit (LSB) comprising:*

*a first driver circuit (958) to drive the LSB by generating an LSB symbol component representing the LSB; and*

*a second driver circuit to drive the MSB by generating an MSB symbol component representing the MSB, the LSB symbol component being combined with the MSB symbol component to provide the output symbol,*

*wherein*

*the first driver circuit (958) includes at least one driver transistor (960-1) and the second driver circuit includes at least one driver transistor (960-3),*

*the first and second driver circuits (958) contain the same number of drive transistors (960), and*

*wherein said at least one driver transistor (960) in one of the first and second driver circuits (958) is twice as large in size as the at least one driver transistor (960) in the other one of the first and second driver circuits, i.e. that a width to length ratio of a respective driver transistor (960) in one of the first and second driver circuits (958) is twice the width to length ratio of a corresponding driver*

*transistor (960) in the other one of the first and second driver circuits,*

*wherein, if the first driver circuit (958) and the second driver circuit (950) each include two or more driver transistors (960-0, 960-1, 960-3, 960-4), then the driver transistors (960-0, 960-1) of the first or second driver circuit have width to length ratios  $W/L$ ,  $2W/L$ , ...,  $2^n W/L$ , and the driver transistors (960-3, 960-4) of the other of the first or second driver circuit have width to length ratios  $2W/L$ ,  $4W/L$ , ...,  $2^{n+1}W/L$ , wherein,*

*in case MSB and LSB are both high or both low, one of the MSB and LSB is driven with twice as much current as the other one of the MSB and LSB, and wherein the first driver circuit and the second driver circuit connect to an I/O pin and output at the I/O pin the sum of the MSB current and the LSB current.*

VII. The appellant's arguments can be summarized as follows:

The object of the invention was to increase the amount of data transferred in each clock cycle, without increasing the number of output pins.

D5 disclosed a differential voltage-mode driver, whereas the invention was directed to a single-ended current-mode driver.

Starting from D5, the skilled person would not have considered converting it to current mode. D5 addressed the problem of a limited number of I/O connections, but proposed a voltage-mode driver. Although current mode transmission was known, it had disadvantages.

Conversion to current mode would have been difficult and have required starting from scratch. Indeed, it would have meant undoing the design choices for the voltage mode driver and making new design choices for current mode. There was no element, at all, of the driver circuit in D5 that corresponded to the driver circuits in the present invention.

The purpose of the transistor stack in D7 was to control the current for adapting to environmental conditions. Those transistors were not driver transistors operating on input data. Therefore, the skilled person would not have considered this document for providing a current mode output driver.

## **Reasons for the Decision**

### 1. *The invention*

The invention concerns a current-mode 4-PAM driver for a multi-drop bus.

The object of the invention is to increase the data rate of the bus without increasing the number of output pins (see the passage bridging pages 9 and 10 in the published application).

4-PAM maps two bits to each output symbol, in contrast to one per symbol for 2-PAM (binary) signalling. Thus, it doubles the data rate without increasing the system clock frequency or the number of output lines; but the signal-to-noise ratio is lower.

The claimed driver provides 4-PAM mapping and driving in current mode, by driving the most-significant bit (MSB) with twice as much current as the least-significant bit (LSB). It may be the other way around, but, for simplicity, the remainder of this decision is written on this basis.

2. *Clarity, support by the description and drawings, and compliance with Article 123(2) EPC*

2.1 The application describes a number of different parts of a bus system (Figure 6), but claim 1 is directed to only one of them, namely the bus output driver described from page 61, line 11 to page 63, line 26, and depicted in Figures 30 and 31. To meet the requirements of Article 84 EPC with respect to clarity and support by the description and drawings, claim 1 must contain all the essential features of this output driver. This has implications also for Article 123(2) EPC, because claim 1 has been restricted to this subject-matter by amendment.

2.2 In the Board's judgment, the skilled person would have understood the invention in figures 30 and 31, and described from page 61, line 9, to page 63, line 26, to be the following:

The output driver has two driver circuits connected in parallel: one provides the current for the MSB, and the other provides the current for the LSB. The drive transistor for the MSB has twice the width-to-length ratio as the drive transistor for the LSB. Consequently, the MSB is driven with twice the current

as the LSB (when they have the same input values - either both high or both low).

The driver output is the sum of the MSB and LSB currents on one pin (956). This is clear from the figures, and from the object of the invention, which includes keeping the number of output pins small.

- 2.3 Each driver circuit may comprise more than one drive transistor. Then, the drive transistors in the first driver circuit have width-to-length ratios  $W/L$ ,  $2W/L$ , ...,  $2^n W/L$ , and the driver transistors in the second driver circuit have width-to-length ratios  $2W/L$ ,  $4W/L$ , ...,  $2^{n+1} W/L$ .

A combination of drive transistors is selected to provide the correct MSB and LSB currents. The same combination is applied to each circuit, so that the MSB current is twice the LSB current.

The selection of drive transistors in the driver circuits, by means of current control bits (CCTRL<6:0>), compensates for environmental factors. Figures 30 and 31 show two ways of doing it, and the application explicitly states that techniques for determining and setting the current control bits are not part of the invention (page 62, lines 1 - 5).

- 2.4 Claim 1 contains all the essential features of the invention as identified above. Therefore, the Board is satisfied that the requirements of Articles 84 and 123(2) EPC are met.



3. *Inventive step*

3.1 The examining division found that the invention as defined in the requests before it lacked inventive step over D5. The Board considers D5 to be a reasonable starting point for the subject-matter of present claim 1, because it concerns a 4-PAM bus driver.

3.2 The driver in D5 is a differential voltage mode driver. It takes inputs A and B and generates as output four voltage levels ( $v_0$ ,  $v_1$ ,  $v_2$ ,  $v_3$ ) on each of two output lines X and Y (figure 3; Table A).

Figure 3 of D5 shows a driver circuit for generating the voltage outputs. Input lead A is connected to a current switch consisting of transistors 203 and 205, and the B input lead is connected to a current switch consisting of transistors 211 and 213. The collectors of transistors 203 and 211 are tied together and connected through a pull-up resistor 221 to the voltage source Vcc. Similarly, the collectors of transistors 205 and 213 are connected together and through pull-up resistor 223 to the source Vcc. A current  $I_a$  is generated for input A, and a current  $I_b$  is generated for input B. When A and B are both 0, the sum of  $I_a$  and  $I_b$  will flow through resistor 223. Similarly, when A and B are both 1,  $I_a + I_b$  will flow through resistor 221. The currents  $I_a$  and  $I_b$  are generated by respective transistors (209 and 227) and resistors (225, 229) connected to voltage source Vee. The value of the resistor 225 is twice that of 229, so that the current  $I_b$  is twice  $I_a$ .

3.3 The output driver of claim 1 differs from D5 in that:

- it operates in current mode, providing the output

level as the sum of the MSB current and the LSB current on one I/O pin; and

- the drive transistor for the MSB has twice the width-to-length ratio of the drive transistor for the LSB.

3.4 The effects of this difference is a reduction of the number of output pins, as well as the effects of current mode over voltage mode transmission. The application does not describe the latter effects, but they are well known (see, for example, D7). One benefit is a reduction of peak switching current, because a current mode driver draws a known current regardless of load and operating conditions. Furthermore, for a current mode driver, no significant impedance discontinuities occur when the driver is in the sending state. As a consequence, reflections are typically avoided and the required bus settling time is decreased.

3.5 The applicant argued that, starting from D5, the skilled person would not have considered converting to current mode. The Board is not persuaded by this argument. The advantages of current mode transmission were well known at the priority date. Therefore, the Board considers that the skilled person would have had the idea of converting the voltage mode driver in D5 to current mode. The question is whether the driver defined by claim 1 would have been an obvious way of doing it.

3.6 D5 contains no teaching as to how to provide 4-PAM signalling in current mode. Therefore, in the Board's view, the skilled person could not have performed this task based on D5 alone. The teaching would have had to come from elsewhere in the prior art.

3.7 The Board is not persuaded by the appellant's argument that the skilled person would not have considered D7, but is satisfied that the teaching of D7 would not have rendered the invention obvious.

In the Board's understanding, D7 discloses a current mode bus driver, which produces a desired output current by turning on or off a particular combination of transistors coupled in parallel (column 3, lines 55 to 66). The widths of those transistors are binary multiples of one another. Thus, D7 discloses the driver circuits as in claim 1, including the arrangement of a plurality of transistors with width-to-length ratios  $W/L$ ,  $2W/L$ , ...,  $2^n W/L$ .

However, D7 does not teach how to use such drivers to provide 4-PAM signalling. In other words, it does not have the two parallel driver circuits, and there is no teaching of how to generate the current for the MSB relative to the LSB. Therefore, the combination of D5 and D7 does not lead to the invention as defined in claim 1.

3.8 Taking D7 as a starting point does not lead to a different conclusion. The skilled person would not have considered a voltage mode driver, such as the one disclosed in D5, when seeking to convert a current mode 2-PAM driver to a current mode 4-PAM driver.

- 3.9 The Board concludes that the subject-matter of claim 1 involves an inventive step (Article 56 EPC).
- 3.10 The Board comes to a different conclusion from the examining division's on inventive step. However, the positive decision on inventive steps is based on features which were not in the claims considered by the examining division, and the Board considers that the examining division was right to refuse the application. Indeed, those claims were not limited to current mode, which is a key feature of the invention.
4. *Length of oral proceedings*
- 4.1 The Board had reserved two days for oral proceedings, in view of the five requests that had to be considered for compliance with Articles 84, 123(2), and 51(2) and 56 EPC.
- 4.2 A few days before the oral proceedings were to take place, the appellant informed the Board by email that all the homebound flights on the second day were fully booked, and that there were almost no hotel rooms available in Munich and expressed a "hope" that the hearing could be finished on one day.
- 4.3 The technical subject matter of the case is, in fact, not terribly complicated as transistor circuits go. The prior art and the issue of inventive step are likewise reasonably straightforward. However, the Board can only consider the requests the appellant lays before it, and must take the time necessary to answer the questions those requests raise. Almost the whole of the oral proceedings were taken up with the comparison of a series of requests with the application as filed. Such

an approach is not consistent with the appellant's desire that proceedings finish in a timely manner.

- 4.4 When oral proceedings are scheduled for more than one day, a party can have no expectation of the hearing being finished on the first of them. If a party does not appear on the second day, the oral proceedings may continue without that party (Rule 115(2) EPC and Article 15(3) RPBA).

## Order

### For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the examining division with the order to grant a patent on the basis of claims 1 to 3 filed as "new request 12.10.17 16:13h" during the oral proceedings (annex I) and a description to be adapted.

The Registrar:

The Chairman:



T. Buschek

P. Scriven

Decision electronically authenticated