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**Datasheet for the decision  
of 7 February 2017**

**Case Number:** T 1497/11 - 3.4.03

**Application Number:** 02797504.4

**Publication Number:** 1466357

**IPC:** H01L21/44, H01L23/047

**Language of the proceedings:** EN

**Title of invention:**

SURFACE MOUNTED PACKAGE WITH DIE BOTTOM SPACED FROM SUPPORT BOARD

**Applicant:**

INTERNATIONAL RECTIFIER CORPORATION

**Headword:**

**Relevant legal provisions:**

EPC 1973 Art. 56  
EPC Art. 52(1), 123(2)

**Keyword:**

Amendments - added subject-matter (yes)  
Inventive step - auxiliary request (yes)

**Decisions cited:**

**Catchword:**



**Beschwerdekammern**  
**Boards of Appeal**  
**Chambres de recours**

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Case Number: T 1497/11 - 3.4.03

**D E C I S I O N**  
**of Technical Board of Appeal 3.4.03**  
**of 7 February 2017**

**Appellant:** INTERNATIONAL RECTIFIER CORPORATION  
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**Representative:** Moore, David Simon  
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**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted on 31 January 2011  
refusing European patent application No.  
02797504.4 pursuant to Article 97(2) EPC.

**Composition of the Board:**

**Chairman** G. Eliasson  
**Members:** S. Ward  
C. Schmidt

## Summary of Facts and Submissions

- I. The appeal is against the decision of the Examining Division refusing European patent application No. 02 797 504 on the ground that the claimed subject-matter did not involve an inventive step within the meaning of Article 56 EPC.
- II. At the end of the oral proceedings held before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 9 of the main request, filed with letter dated 6 December 2010 or, alternatively, in the following version (auxiliary request):
- claims 1 to 8 filed at the oral proceedings before the Board,
  - description pages 1, 2, 2a, 3 and 5 filed at the oral proceedings before the Board, pages 4 and 6 as published,
  - drawings: sheets 1/2 and 2/2 as published.
- III. The following documents are referred to in this decision:
- D1: US 6 262 489 B2  
D3: US 2001/0048116 A1  
D4: Microelectronics Packaging Handbook,  
Tummala, Rymaszewski (1988),  
pages 366-369.
- IV. Claim 1 of the main request reads as follows:
- "A semiconductor device package (24) comprising:  
a semiconductor device die (10) having a first surface  
substantially parallel to a second surface;*

*said first surface having a first solderable planar metal electrode;*  
*said second surface having a second solderable planar metal electrode (18, 20);*  
*a metallic conductive clip (12) having a flat web portion, said web portion having a first surface and a second surface, said second surface of said web portion being electrically connected with said first electrode;*  
*and*  
*at least one electrical connector (22) comprising a solderable planar metal post-shaped electrode extending from an edge of said web portion over and spaced from an edge of said semiconductor device die (10) and terminating at a connection surface, wherein said semiconductor device die (10) is inwardly recessed such that said second electrode (18, 20) of said semiconductor device die (10) is not flush with said connection surface, and said connection surface is adapted to mount to a metallized pattern on a support surface,*  
*wherein said semiconductor device die (10) is inwardly recessed between 0.001 and 0.005 inches (25.4 and 127  $\mu$ m)."*

Claim 1 of the auxiliary request comprises the entire text of claim 1 of the main request, plus the following amendment (in bold):

*"... wherein said semiconductor device die (10) is inwardly recessed **in the interior of said clip** such that ..."*

V. The findings of the Examining Division, insofar as they are relevant to the present decision, may be summarised as follows:

Document D1 was the closest prior art and disclosed all features of claim 1 apart from the amount of the recess. The Figures in D1 are schematic and could not be used to infer the amount of recess of the die 18. Consequently it was necessary to consider objectively the disclosure of D1 as a whole in order to ascertain the size of the recess.

By considering the method of forming the assembly, the conclusion for the skilled reader would be that the die 18 in the final assembly remained substantially in its initial position, and consequently the planar metal electrode ("bond pad") of the die 18 must be recessed compared to the plane of the connecting surfaces of legs 32 of contact member 20 by approximately the diameter of the solder bumps 42.

The skilled person would know that solder bumps for an integrated circuit die typically had diameters of from about 25µm - 125µm. This view was supported by extracts from the Handbook D4. Consequently the skilled person following the teaching of D1 and providing solder bumps of a diameter typical for the technical field would automatically arrive at the subject-matter of claim 1 without an inventive step.

Furthermore, the requirements of Article 123(2) EPC were not met as a result of the omission in claim 1 of the feature that the semiconductor die is recessed in the interior of the clip (as in original claim 1).

VI. The appellant's arguments, insofar as they are relevant to the present decision, may be summarised as follows:

Within the context of claim 1 of the main request, the omission of the feature "in the interior of said clip

did not alter the meaning of the claimed subject-matter, and hence did not result in the requirements of Article 123(2) EPC not being met.

Document D1 was the closest prior art, with claim 1 differing in that the semiconductor device die was inwardly recessed between 0.001 and 0.005 inches (25.4 $\mu$ m and 127 $\mu$ m). This had the technical effect of reducing failure due to thermal cycling. This difference was neither suggested by D1 alone nor by a combination of documents D1 and D4.

Moreover, claim 1 defined a semiconductor device package, whereas document D1 disclosed a method and assembly for mounting a semiconductor IC device to a substrate using flip chip technology, which was not the same thing.

Furthermore, starting from the package of Figs. 20 and 21 of document D3, the skilled person would not look to document D1 which dealt with an IC flip chip assembly. In any event, there was no clear teaching in document D1 that stress relief from thermal cycling was achieved merely by recessing the die, rather it appeared to be the underfill material 40 which promoted such stress relief.

## **Reasons for the Decision**

1. *Article 123(2) EPC*
- 1.1 In section III ("Additional Matters") of the contested decision, the Examining Division found that the requirements of Article 123(2) EPC were not met as the

phrase "in the interior of the clip", which was present in claim 1 as originally filed, was absent from claim 1 of the application as refused.

- 1.2 In claim 1 as originally filed, a device was defined in which a semiconductor device die was inwardly recessed in the interior of a clip. This left no room for doubt that the phrase "inwardly recessed" referred to the location of the semiconductor device die within the clip.

In claim 1 of the present main request, the phrase "in the interior of said clip" is omitted. As a result, this claim - while still covering embodiments in which the location of the die within the clip is being referred to - must now be seen as including additional embodiments, for example embodiments in which "inwardly recessed" refers to the form of the semiconductor device die, rather than its location. Such embodiments do not have a basis in the original application as filed, and hence claim 1 of the main request does not meet the requirements of Article 123(2) EPC.

- 1.3 In claim 1 of the auxiliary request, the phrase "in the interior of the clip" has been restored, and the Board has no other objections in this respect. Hence, the auxiliary request is found to meet the requirements of Article 123(2) EPC.

2. *Clarity (Article 84 EPC 1973)*

The clarity issues raised during examination (in relation to the terms "clip" and "web") were not pursued in the contested decision, even in the "additional Matters", and the Board sees no reason to raise objections under Article 84 EPC 1973.



3. *Auxiliary request: inventive Step starting from D1*

3.1 The Examining Division found that the claimed subject-matter differed from the disclosure of document D1 only in the depth of the inward recess ("between 0.001 and 0.005 inches (25.4 and 127  $\mu\text{m}$ )."

The Board, however, sees a further difference.

3.2 Claim 1 is directed to a semiconductor device package. The skilled person would understand the term "package" to mean a product comprising a number of individual components which are mechanically integrated into a single unit.

According to claim 1, the component features of the package are:

- a semiconductor device die;
- a metallic conductive clip having a flat web portion; and
- at least one electrical connector extending from an edge of the web portion.

The remainder of the claim defines further details of these features and their interrelationships.

3.3 One such detail is that the electrical connector comprises a solderable planar metal post-shaped electrode which terminates at a connection surface, the connection surface being adapted to mount to a metallized pattern on a support surface.

This feature represents a functional constraint on the connection surface, i.e. it must be such as to allow mounting to a metallized pattern on a support surface.

The support surface is not, however, part of the claimed package.

- 3.4 Document D1 discloses a "method and assembly for mounting an IC semiconductor device to a substrate using flip chip technology" (see abstract). Fig. 2 shows the components in an unassembled state, prior to registration and soldering, including a chip 18 (corresponding to the claimed semiconductor device die), a contact member 20 (corresponding to the claimed metallic conductive clip) and a substrate 20 (corresponding to the support surface to which the claimed package must be mountable).

Proceeding by the series of manufacturing steps set out in document D1, the assembled product depicted in Figs. 1 and 3 is formed.

- 3.5 The product disclosed in document D1 does not correspond to that claimed in the present application, as it is not a package with connection surfaces being adapted to mount to a metallized pattern on a support surface, but rather an assembly which is already mounted to a support substrate 12 as depicted in Figs. 1 and 3.

Nor is there any intermediate stage disclosed or implied in which the elements of the assembly other than the substrate could be said to form a package adapted to be mounted on the substrate, as defined in claim 1.

In fact, the manufacturing process disclosed is an essentially continuous process, in which the solder bumps 42 and the solder 44 melt first during reflow, and further heating then causes the solder 46 between

the chip 18 and contact member 20 to reflow. At no stage is any product brought into existence which could be identified with the package of claim 1.

- 3.6 Document D1 does not, therefore, disclose a semiconductor device package of the claimed type, and hence this represents a further feature distinguishing the claimed subject-matter from this prior art.
- 3.7 To adapt the assembly disclosed in document D1 to arrive at the subject-matter of claim 1, the skilled person would not only have to select an amount of recess corresponding to that claimed (as set out in the contested decision), but would also have to modify the process so that the final product (or at least an intermediate product) would correspond to the claimed package, i.e. a unit comprising chip 18 attached to contact member 20 with connection surfaces adapted to mount to (but not yet mounted to) the support surface 12.
- 3.8 Far from being obvious, such modifications would amount to creating a new invention fundamentally different to that disclosed in document D1. The Board therefore concludes firstly that the skilled person would not arrive in an obvious manner at the subject matter of the claimed invention starting from document D1, and secondly that document D1 is not a suitable choice for the closest prior art.

4. *Auxiliary request: inventive Step starting from D3*

- 4.1 The Board considers the closest prior art to be that set out in the embodiment of Figs. 20 and 21 and paragraphs [0049] and [0050] of document D3. This prior

art is also shown in Figs. 1 and 2 of the present application and discussed in the description.

4.2 Document D3 discloses a semiconductor device package comprising a semiconductor device die (30); a metallic conductive clip (100) having a flat web portion; and electrical connectors terminating at connection surfaces (105) adapted to mount to a metallized pattern on a support surface (paragraph [0050]). It is immediately apparent that all features of claim 1 are disclosed in this embodiment with the exception of the following:

- *wherein said semiconductor device die is inwardly recessed in the interior of said clip such that said second electrode of said semiconductor device die is not flush with said connection surface; and*
- *wherein said semiconductor device die is inwardly recessed between 0.001 and 0.005 inches (25.4 and 127  $\mu$ m).*

4.3 Having regard to this prior art, the problem formulated in the description of the present application is reducing temperature cycling failures, and the Board sees no reason to differ. The question is therefore whether the skilled person would find it obvious, on the basis of the prior art and common general knowledge in the field, to incorporate the distinguishing features into the embodiment of Figs. 20 and 21 of document D3 in order to solve this problem.

4.4 Fig. 21 of document D3 depicts the upper electrode of the die as being coplanar with the connection surfaces (105). This is not a mere artifact of a schematic drawing, as confirmed in paragraph [0050]:

- *"The top surface of solderable contact 40 is coplanar with drain clip projection surfaces 105. Thus, all of contacts 105, 40 and 37 will align with contact traces on a printed circuit board."*

The upper surface of the electrode 40 being flush with the connection surface 105 is therefore a feature of this embodiment which has been selected for a specific technical purpose. For this reason alone, it is questionable whether the skilled person would consider tampering with this aspect of the closest prior art.

- 4.5 In document D1 the problem of relieving stress provoked by thermal cycling is mentioned, and it was discussed in oral proceedings whether the combination of these two documents would lead the skilled person to the claimed invention.

In the embodiment of Figs. 20 and 21, document D3 discloses a vertical power MOSFET (see paragraph [0036]), in which "the die of FIGS. 7 and 8 is mounted in a cup-shaped clip 100". The upper electrode 40, which is destined to be mounted to a printed circuit board, is a source contact in the form of a "large area solderable contact", and the bottom electrode is a drain contact 34 (see paragraphs [0041] and [0050], Figs. 7, 8, 20 and 21).

Document D1, on the other hand, discloses an integrated circuit flip chip arrangement in which the chip is provided with bond pads on which solder bumps are formed. Bonding involves registering the solder bumps with a conductor pattern on a printed circuit board, and reflow soldering the solder bumps. The finished bond comprises "columnar solder connections 22", with

the gaps between them being filled with underfill material 40, as shown in Fig. 3.

4.6 The disclosures of documents D3 and D1 are therefore quite different in terms of the types of the semiconductor devices (power MOSFET as opposed to IC) and the connecting arrangements to the substrate (large area solderable contact as opposed to an array of solder bumps leading to columnar solder connections with underfill material between them). For this reason, the Board finds it implausible that a skilled person would look to document D1 for solutions to problems arising in relation to the embodiment of Figs. 20 and 21 of document D3.

4.7 Moreover, even supposing *arguendo* that a combination of these documents came into consideration, the skilled person would not regard the solution proposed in document D1 as being applicable to the arrangement of document D3.

4.8 In document D1, the spacing between a flip chip and its substrate is mentioned in connection with stress relief during thermal cycling as follows:

- *"Sufficient spacing between a flip chip and its substrate, known as the "stand-off height," is desirable for enabling stress relief during thermal cycles, allowing penetration of cleaning solutions for removing undesirable processing residues, and enabling the penetration of mechanical bonding and underfill materials between the chip and its substrate. As such, the assembly method of this invention promotes the life of the flip chip assembly by helping to control the final height of*

*the first solder connections." (column 2, lines 42-50.)*

- *"... the contact member 20 achieves sufficient spacing between the chip 18 and substrate 12, which allows penetration of cleaning solutions for removing undesirable processing residues after reflow, enables the underfill material 40 to completely penetrate and fill the gap between the chip 18 and substrate 12, and promotes stress relief during thermal cycling" (column 5, lines 10-16..*

Whilst perhaps not entirely clear, these passages appear to point to the underfill material being the key element in promoting stress relief during thermal cycling, with the "sufficient spacing" appearing to refer to the provision of a gap between the die and the substrate which is sufficient to facilitate this underfilling.

4.9 This interpretation is further reinforced by the following passage:

- *"FIG. 3 also shows the chip 18 as being underfilled with a suitable underfill material 40, as is well known in the art for promoting the thermal cycle life of the solder connections 22 ... The contact member 20 particularly does not interfere with underfilling the corners of the chip 18, for which uniform underfilling can be more critical due to there often being higher stresses at the corners during thermal cycling." (column 4, lines 34-44.)*

4.10 The skilled person would therefore derive from document D1 a technique for reducing stress during thermal

cycling which includes, as a key element, the provision of an underfill material located between the chip and the substrate, and which fills the gaps between adjacent columnar solder connections, as well as any gaps between the the columnar solder connections and the corners of the die.

- 4.11 In the embodiment of Figs. 20 and 21 no gaps suitable for underfilling are disclosed, nor is it likely that they would arise after soldering the package to a substrate. The upper (source) electrode 40 is a "large area solderable contact", and the Board presumes that the intention would be to use essentially the entire "large area" of this solderable contact for soldering (otherwise why provide a large area?). In the final mounted product the source contact 40 would therefore be in mechanical and electrical contact with the substrate by means of a solder layer extending over essentially the entire "large area" of the contact. There would be no gaps suitable for implementing the solution proposed in document D1.
5. The Board therefore concludes that the skilled person would not find the invention defined by the auxiliary request to be obvious in the light of the prior art, and hence the subject-matter of claim 1 of the auxiliary request filed at oral proceedings before the Board is judged to involve an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.



## Order

### For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the department of first instance with the order to grant a patent in the following version:
  - claims 1 to 8 filed at the oral proceedings before the Board,
  - description pages 1, 2, 2a, 3 and 5 filed at the oral proceedings before the Board, pages 4 and 6 as published,
  - drawings: sheets 1/2 and 2/2 as published.

The Registrar:

The Chairman:



S. Sánchez Chiquero

G. Eliasson

Decision electronically authenticated