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Datasheet for the decision of 2 March 2017

Case Number: T 1489/11 - 3.5.06

Application Number: 07869086.4

Publication Number: 2092423

IPC: G06F9/445, H03K3/037

Language of the proceedings: EN

Title of invention:
MAINTAINING INPUT AND/OR OUTPUT CONFIGURATION AND DATA STATE DURING AND WHEN COMING OUT OF A LOW POWER MODE

Applicant:
Microchip Technology Incorporated

Headword:
Low power mode/MICROCHIP

Relevant legal provisions:
EPC 1973 Art. 56
EPC R. 103(1)(a)

Keyword:
Inventive step - (no)
Substantial procedural violation - (no)

Decisions cited:

Catchword:

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Case Number: T 1489/11 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 2 March 2017

Appellant: (Applicant)	Microchip Technology Incorporated 2355 West Chandler Boulevard Chandler, AZ 85224-6199 (US)
Representative:	Grubert, Andreas c/o Westphal, Mussgnug & Partner Patentanwälte mbB Herzog-Wilhelm-Straße 26 80331 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 23 February 2011 refusing European patent application No. 07869086.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	W. Sekretaruk
Members:	A. Teale
	G. Zucka

Summary of Facts and Submissions

I. This is an appeal against the decision, dispatched with reasons on 23 February 2011, to refuse European patent application No. 07 869 086.4 on the basis that there was no agreed text of the application. Amended claims according to a main and an auxiliary request (referred to as the "ultimate requests" below) submitted by the applicant before the oral proceedings, which were subsequently not attended by the applicant, were not admitted by the examining division into the proceedings, Rule 137(3) EPC, on the basis that they were late-filed and that *prima facie* the independent claims of both requests did not comply with Article 123(2) EPC and the independent claims of the auxiliary request were unclear, Article 84 EPC.

II. In the course of examination proceedings the examining division raised a novelty objection based on the following document:

D4: EP 1 098 239 A1.

III. The first instance proceedings, from the summons to oral proceedings onwards, may be summarized as follows. On 30 August 2010 the examining division issued a summons to oral proceedings and indicated in an annex that it maintained objections previously raised and that any amendments should be filed no later than one month before the date of the oral proceedings, in other words by 8 January 2011. On 18 November 2010 the applicant responded by filing arguments and amended claims according to new main and auxiliary requests. These are referred to below as the "penultimate requests". On 18 January 2011 the examining division raised clarity objections against the claims of both

requests. On 24 January 2011 the applicant responded by filing arguments and amended claims according to main and auxiliary requests, referred to below as the "ultimate requests". The applicant did not attend the subsequent oral proceedings at which the examining division took the appealed decision.

IV. A notice of appeal was received on 21 April 2011, and the appeal fee was paid on the same day.

V. With a statement of grounds of appeal, received on 21 June 2011, the appellant filed amended claims according to main and auxiliary requests to replace all requests currently on file. The appellant requested grant of a patent based on the main or auxiliary requests and otherwise oral proceedings. The appellant also alleged that a substantial procedural violation had taken place and requested reimbursement of the appeal fee, Rule 103(1)(a) EPC.

VI. In an annex to a summons to oral proceedings the board introduced a new document, Article 114(1) EPC 1973:

D6: "MCS51 Microcontroller Family User's Manual", Order No. 272383-002, Intel Corporation, February 1994, pages i to iii and 5-7 to 5-10, downloaded from the URL http://datasheets.chipdb.org/Intel/MCS51/MANUALS/27238302.PDF on 18 November 2016.

and set out its preliminary opinion that the application complied with Article 123(2) EPC regarding added subject-matter. The board however expressed doubts as to the clarity of the claims, Article 84 EPC 1973, and inventive step, Article 56 EPC 1973, in view of D4 and common general knowledge exemplified by D6. The board also expressed its preliminary opinion that

no substantial procedural violation, Rule 103(1)(a) EPC, or fundamental procedural deficiency, Article 11 RPBA, had occurred.

VII. With a submission received on 2 February 2017 the appellant filed amended claims according to new main and auxiliary requests.

VIII. At the end of the oral proceedings held on 2 March 2017 the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request or on the basis of the auxiliary request, both filed on 2 February 2017. The appellant further requested that the appeal fee be reimbursed. After deliberation, the board announced its decision.

IX. The application is being considered in the following form:

Description (both requests):
pages 1 to 12, received on 12 June 2009.

Claims (all received on 2 February 2017):
Main request: 1 to 15
Auxiliary request: 1 to 15.

Drawings (both requests):
Pages 1/5 to 5/5, as originally filed.

X. Claim 1 according to the main request reads as follows:

"An integrated circuit device having a low power mode and maintained external input and/or output configuration and data states, comprising:

a plurality of logic circuits (132); and

an input and/or output node (104; 204; 304) coupled to the plurality of logic circuits (132), wherein the plurality of logic circuits (132) control the configuration and data state of said input and/or output node (104; 204; 304) during normal power mode, the input and/or output node (104; 204; 304) comprises an input and/or output keeper cell (106; 206; 306) coupled to a configurable output driver (108; 208) and being controllable to drive an external output (112, 212, 312) and/or a configurable input receiver (110; 310) receiving an input signal from an external input (112, 212, 312);

wherein when the input and/or output keeper cell (106; 206; 306) receives an enter low power mode signal the input and/or output keeper cell (106; 206; 306) will latches [sic] in the input receiver and/or output driver data state and respective configuration of said configurable input receiver (110; 310) and/or output driver (108; 208);

wherein when the input and/or output keeper cell (106; 206; 306) receives a wake-up and restore from low power mode signal the input and/or output keeper cell (106; 206; 306) ceases to latch in and returns control of the input receiver and/or output driver data state and configuration of the input receiver (110; 310) and/or output driver (108; 208) configuration to the plurality of logic circuits (132), and

a low power mode register (134), which during low power mode remains operational while said plurality of logic circuits (132) are put into low power mode, wherein said low power mode register (134) controls the enter low power mode signal and the wake-up and restore from

low power mode signal, said low power mode register (134) being coupled with said input and/or output keeper cell (106; 206; 306) and said plurality of logic circuits (132) and wherein the low power mode register (134) generates said wake-up and restore from low power mode signal only after internal logic levels of said plurality of logic circuits (132) controlling said configuration and data state of said input and/or output node (104; 204; 304) have been re-established to the state before the low power mode has been entered."

The claims according to the main request also comprise a corresponding independent method claim 12.

XI. Claim 1 according to the auxiliary request differs from that of the main request in the restriction of the expression "internal logic levels" to read "all internal logic levels" and in the feature at the end that "the integrated circuit device is configured to read the state of said input and/or output keeper cells (106; 206; 306) by software or firmware to re-establish their internal logic levels".

The claims according to the auxiliary request also comprise a corresponding independent method claim 11.

Reasons for the Decision

1. The admissibility of the appeal

The appeal complies with the admissibility criteria under the EPC and is consequently admissible.

2. Technical summary of the invention

2.1 The invention relates to integrated circuit devices which maintain their external input/output (I/O) configuration and data states when they are put into a low power mode and subsequently brought out of it again.

2.2 The description acknowledges prior art devices which perform a "power-on reset" on exiting from a low power mode, meaning that "keeper cells", used to retain the I/O configuration and data states in the low-power mode by latching data, may be reset into a default, or even an unknown, state, causing the device to possibly disturb other connected devices; see page 1, lines 6 to 30.

2.3 The invention seeks to bring a device out of a low-power mode and restore the I/O configuration and data states without disturbing other connected devices. Figure 1 illustrates an integrated circuit device (102) comprising logic circuits (132), a low power mode register (134) and a configurable I/O node (104), meaning that the node can act as an input only, an output only or as a bidirectional I/O node. The I/O node is connected to external circuitry (112) and comprises an I/O keeper cell (106), an output driver (108) and an input receiver (110). In the low power mode the device logic circuits (132) are not supplied with power, but power is supplied to the low power mode register and the I/O node.

2.4 According to page 6, lines 9 to 19, as the device comes out of the low power mode the plurality of logic circuits performs a systematic, well-defined sequence for waking up and for establishing proper logic levels

on all internal signal paths. Only then is a signal sent from the lower power mode register (134) on the "wake-up and restore from low power mode" signal line 116 to the I/O keeper cell causing it to "cease to latch-in (store, retain, *etc*.) the last I/O configuration and data logic level(s) [and] ... become transparent again between circuits in the configurable node 104 (e.g. driver 108 and/or receiver 110), and the data-out signal line 118 and/or data-in signal line 120 and the I/O configuration and data states signal line 130." Beyond this functional definition, the application provides no further details of the keeper cells, in particular their internal structure.

3. Document D4

3.1 D4 relates to reducing the power consumption of a microcontroller by shutting down its core logic, the part of the microcontroller consuming the most power, while maintaining input-output (I/O) port integrity, meaning that the core logic is powered down, but the I/O port logic remains powered up and in the same state; see title and abstract.

3.2 As illustrated in figure 1, the integrated circuit microcontroller (100) comprises core logic (114), connected by a power switch (110) to the power source (108). The core logic is connected via interface logic (104) to I/O port logic (106) which is permanently connected to the power source and comprises latches (116) connected to external outputs (118) as well as external inputs (120); see paragraph [0022], lines 40 to 49. The I/O port logic controls the power switch and thus the provision of power to the core logic. The logic levels of the outputs (118) of the I/O port logic may be stored in registers or latches (116), thus

maintaining the most recent logic state of the outputs (118) of the I/O port logic when power is removed from the core logic; see paragraph [0025], lines 16 to 20.

3.3 Figures 2 and 3 illustrate the power-down and power-up sequences, respectively. When powering down, the core logic causes the clock inputs to the interface logic and/or I/O port logic to be disabled (step 204). Then the core logic causes its outputs to be disconnecting from the interface logic and/or the I/O port logic (step 206). Finally power is turned off to the core logic (step 208). The power-up sequence mirrors the power-down process.

3.4 In the annex to the reasons for the appealed decision the examining division stated that D4 represented the closest prior art and that it regarded the core logic (102) in D4 as the claimed "plurality of logic circuits". The I/O port logic 106 including the output latches 116 was regarded as the claimed "input and/or output node" having an "input and/or output keeper cell" coupled to a "configurable output driver driving an "external output" (118) and/or a configurable input receiver receiving an input signal from an external input (120). The examining division concluded that the subject-matter of claim 1 differed from the disclosure of D4 in explicitly setting out a "low power mode register" to drive the power down/power up signals. The appellant has argued that the annex does not consider the features of the characterizing part of claim 1.

3.5 The board accepts that D4 forms the closest prior art on file, but finds that D4 does not disclose as many features of claim 1 as was stated in the annex to the appealed decision. Claim 1 of both requests sets out three options: an input and output (bidirectional) node

(see figure 1), an output only node (see figure 2) and an input only node (see figure 3). The disclosure of D4 comes closest to the output node option. Whilst the board regards an output driver to be implicit in the disclosure of D4, D4 does not disclose a "configurable" input/output node or a "configurable" output driver".

3.6 The appellant argued in the submission of 2 February 2017 and in the oral proceedings that the latches 116 in D4 were passive, had only two states and could not be regarded as the keeper cells set out in claim 1, since keeper cells were more active and could not only act as latches but could also become "transparent" (see page 6, lines 12 to 18), expressed in claim 1 as returning control of the output driver data state to the plurality of logic circuits. The board notes that a latch, for instance the latches 116 in D4, can be made to behave transparently by clocking it. Indeed the board understands such clocking of the latches 116 in D4 to be implicit in order that the output signals 118 follow the core logic when the device is "awake". Hence the board finds that the latches 116 in D4 can, for the claimed case of an output node, be regarded as an output "keeper cell" in the sense of claim 1. The board sees no reason to assume that the claimed keeper cells have more than two states. At the oral proceedings the appellant argued that the expression on page 1, line 23, "standard input-output (I/O) "keeper" cells" should not be understood as an admission that keeper cells were known in the prior art. That was why quotation marks had been used around "keeper". Given the functional definition of keeper cells in the application, the board finds that the claimed function is provided in the device of D4 by the latches 116.

3.7 Hence the board takes the view that D4 discloses the following features of claim 1 according to the main request, understood according to the output node option: an integrated circuit device (see abstract, first sentence, "integrated circuit") having a low power mode (see abstract, first sentence, "may be powered down") and maintained external output configuration (outputs remain outputs in D4) and data states (see title and abstract, first sentence), comprising a plurality of logic circuits (core logic 102) and an output node (port logic 106) coupled (via interface logic 104) to the plurality of logic circuits (102), wherein the plurality of logic circuits control the data state of said output node during normal power mode, the output node comprising an output keeper cell (latches 116) coupled to an output driver and being controllable to drive an external output (118), wherein the output keeper cell is adapted to latch in the output driver data state (see figure 2; steps 204 and 206) and to cease to latch in and return control of the output driver data state to the plurality of logic circuits.

3.8 Hence the subject-matter of claim 1, for the output node option, differs from the disclosure of D4 in the following features:

i. the plurality of logic circuits control the configuration, i.e. input only, output only or bidirectional, of the node in the normal power mode;

ii. the output driver is configurable;

iii. when the output keeper cell receives an "enter low power mode" signal the keeper cell latches in

the output driver data state and respective configuration of said configurable output driver;

iv. when the output keeper cell receives a "wake-up and restore from low power mode" signal the output keeper cell ceases to latch in and returns control of the output driver data state and configuration of the output driver to the plurality of logic circuits and

v. a low power mode register, which during low power mode remains operational while said plurality of logic circuits are put into low power mode, wherein said low power mode register controls the "enter low power mode" signal and the "wake-up and restore from low power mode" signal, said low power mode register being coupled with said output keeper cell and said plurality of logic circuits and

vi. wherein the low power mode register generates said "wake-up and restore from low power mode" signal only after internal logic levels of said plurality of logic circuits controlling said configuration and data state of said output node have been re-established to the state before the low power mode was entered.

3.9 Regarding the features added to claim 1 of the auxiliary request with respect to that of the main request, namely:

vii. re-establishing all internal logic levels (based on page 8, line 7) and

viii. the integrated circuit device being configured to read the state of said output keeper cells by software or firmware to re-establish said internal logic levels (based on page 6, lines 20 to 23),

the board takes the view that feature "vii" is not directly and unambiguously derivable from D4. Feature "viii" is however implicit in the operation of the latches (figure 1; 116) in D4 and therefore not a difference feature with respect to D4.

4. Inventive step, Article 56 EPC 1973

4.1 The main request

4.1.1 In the annex to the appealed decision the examining division stated that, even if D4 did not explicitly disclose a "low power mode register" that "generates the wake up and restore from the low power mode signal", it was clearly disclosed that "the entering into low power mode" could be initiated by the microcontroller; see figure 2; step 202 and paragraph [0027], lines 42 to 44. It was implicit from the disclosure of D4 that the "power down/power up signals" were controlled by bits stored in registers. Hence the skilled person, starting from the IC of D4 would implement such a "low power mode register" to store the bits that control "a wake-up and restore from the low power mode signal" and thus arrive at the subject-matter of claim 1 without inventive skill. The same arguments applied to claim 1 of the auxiliary request.

4.1.2 In the submission received on 2 February 2017 the appellant argued that the object of the present invention was to increase power savings while keeping

external devices of a microcontroller operational during a low power mode. Conventional microcontrollers kept entire I/O ports operational during a sleep mode while shutting down the internal core. The invention only kept a minimal part of the I/O port operational, thus increasing power savings. The board notes that the appellant's arguments relate to the interface logic (104) which is distinct from the I/O port logic (106) in D4 and is not set out in the claims. At the oral proceedings the board invited the appellant to indicate those elements of the I/O port in the D4 device that would not be powered in the low power mode in the device according to the invention. The appellant was unable to do so and withdrew this line of argument.

4.1.3 The board takes the view that the difference features between the subject-matter of claim 1 and the disclosure of D4 can be partitioned into three groups, each group addressing an unrelated technical problem. Hence inventive step must be considered separately for each group of features.

4.1.4 Difference features "i" and "ii" relate to the problem of configuring the interface between the integrated circuit device and the outside world. The board takes the view that such configuration options were usual in microcontrollers at the priority date. They were, for instance, already present in the widely used 8051 microcontroller, described in D6. Regarding feature "i", the device ports in D6 are bidirectional (see page 5-7, left column, lines 1 to 3), but may also be used as inputs or outputs; see page 5-8, left column, lines 7 to 10. Turning to feature "ii", figures 3 and 4 illustrate the use of pFETs (P1-P3) as configurable pull-up elements at the pins of ports 1, 2 and 3, port 0 having open drain outputs; see page 5-8, left column,

lines 6 to 7, and page 5-9, left column, lines 6 to 9. The appellant has not challenged these arguments, set out in the annex to the summons to oral proceedings.

4.1.5 Difference features "iii" and "iv" relate to the problem of latching data and configuration and set out the use of certain, arbitrarily named, signals to control the output keeper cell to latch data in the usual way. The use of a keeper cell to latch data in this manner is regarded as a usual matter of design for the skilled person. The skilled person would also recognise that the configuration of the output driver in D4 must not change as a result of entering and leaving a low power mode, and the use of the latches 116 to preserve the output driver configuration would have been a straightforward solution for the skilled person.

4.1.6 Features "v" and "vi" relate to the problem of controlling the integrated circuit as it enters and leaves the low power mode, this problem already being addressed in D4. They set out the "low power mode register" which is always powered and is connected to the logic circuits and also generates two control signals (power-down, wake-up) for the output keeper cell. They also set out the use of the "wake-up" control signal to make the keeper cell become "transparent" again once the logic circuits have been restored on leaving the low power mode. The board finds that the skilled person implementing the microcontroller of D4 would have used a register to implement such control arrangements without inventive skill. It would also have been a usual design choice to only make the keeper cell "transparent" once the logic circuits had been restored; to do otherwise would fail to maintain "input-output port integrity", as the title

of D4 puts it. Hence these features are unable to lend inventive step to claim 1.

4.2 The auxiliary request

4.2.1 Regarding difference feature "vii", the appellant argued at the oral proceedings that it was implicit in the application that registers in the integrated circuit device stored internal logic levels in the low power mode.

4.2.2 The board finds that feature "vii" merely sets out re-establishing all internal logic levels instead of only some, when leaving the low power mode. The board regards re-establishing all internal logic levels as a matter of usual design for the skilled person which is unable to lend inventive step to claim 1.

4.3 Summary on inventive step

The subject-matter of claim 1 of both requests does not involve an inventive step, Article 56 EPC 1973, in view of D4 and the common general knowledge of the skilled person, in particular as exemplified by D6.

5. The alleged substantial procedural violation

5.1 The appellant has argued that the examining division committed a substantial procedural violation, Rule 103(1)(a) and Article 125 EPC, in its finding that the result of not admitting the main and auxiliary requests (the "ultimate requests") received on 24 January 2011 was that there was no text of the application agreed by the applicant. The appellant did not explain the relevance of Article 125 EPC, which concerns principles of procedural law generally recognised in the

contracting states, to his arguments, and the board can see no relevance either. According to the appellant, the examining division had erred in assuming that, by filing the ultimate requests, the applicant had withdrawn the penultimate requests. The appellant pointed out that the letter accompanying the ultimate requests contained no statement withdrawing the penultimate requests and argued that, if at all, the penultimate requests should have been interpreted as "further auxiliary requests". In the appellant's view, the examining division was partly responsible for the ultimate requests being late-filed, since, although the penultimate requests had been filed almost two months before the deadline set for further submissions, namely one month before the oral proceedings, the examining division had only raised clarity objections against the penultimate requests after the deadline had passed. Thus the examining division seemed to have "intentionally deprived Applicant of any possibility to correct any deficiencies". Moreover the examining division had been inconsistent in not admitting the ultimate requests as late-filed, yet accepting the accompanying letter as withdrawal of the penultimate requests, which ran contrary to the principle of "equity and good faith", according to which the examining division should have ignored the entire submission as late-filed.

5.2 In the board's view, the procedural position when the ultimate requests were filed was clear to the applicant. The board sees no contradiction between regarding the ultimate requests as replacing the penultimate ones and then not admitting the ultimate requests as not complying with Articles 84 and 123(2) EPC, as foreseen in Article 114(2) EPC. The examining division was entitled, as is usual practice at the EPO,

to regard the ultimate requests as replacing the penultimate requests or, put another way, as an implicit withdrawal of the penultimate requests. The board sees no reason why the examining division should have, contrary to Article 113(2) EPC 1973, ignored the applicant's labelling of the ultimate requests as "Main request" and "Auxiliary request" (and corresponding statements in the accompanying letter) and instead have considered them as "Second auxiliary request" and "Third auxiliary request", respectively. If that had been the applicant's intention, then he should have labelled his ultimate requests accordingly. Alternatively, the applicant could have stated in the accompanying letter that the penultimate requests were maintained if the ultimate requests were not admitted into the proceedings. Although, in view of the imminent oral proceedings, the examining division was not obliged to issue another communication after the summons to oral proceedings, it did in fact do so in the form of the communication dated 18 January 2011, raising clarity objections against the penultimate requests. Hence the appellant cannot derive rights from the date on which he received said communication. The applicant subsequently chose not to attend the oral proceedings at which he could have defended, or possibly, with the permission of the examining division, replaced, the ultimate requests.

5.3 Consequently the board finds that no procedural violation, let alone a substantial procedural violation, Rule 103(1)(a) EPC, or a fundamental procedural deficiency, Article 11 RPBA, occurred.

Order

For these reasons it is decided that:

1. The appeal is dismissed.
2. The request for reimbursement of the appeal fee is refused.

The Registrar: The Chairman:

B. Atienza Vivancos W. Sekretaruk

Decision electronically authenticated