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Datasheet for the decision
of 13 June 2014

Case Number:	T 1460/11 - 3.5.05
Application Number:	09157010.1
Publication Number:	2107745
IPC:	H04L25/49, H03M1/08
Language of the proceedings:	EN

Title of invention:
Method and system for bit polarization coding

Applicant:
Linear Technology Corporation

Headword:
2's complement A/D coding with bit polarization coding/LINEAR
TECHNOLOGY

Relevant legal provisions:
EPC Art. 56

Keyword:

Decisions cited:

Catchword:

Case Number: T 1460/11 - 3.5.05

D E C I S I O N
of Technical Board of Appeal 3.5.05
of 13 June 2014

Appellant: (Applicant)	Linear Technology Corporation 1630 McCarthy Boulevard Milpitas, CA 95035-7417 (US)
Representative:	Müller-Boré & Partner Patentanwälte PartG mbB Friedenheimer Brücke 21 80639 München (DE)
Decision under appeal:	Decision of the Examining Division of the European Patent Office posted on 18 January 2011 refusing European patent application No. 09157010.1 pursuant to Article 97(2) EPC.

Composition of the Board:

Chair	A. Ritzka
Members:	P. Cretaine
	D. Prietzel-Funk

Summary of Facts and Submissions

I.   This appeal is against the decision of the examining
        division announced in oral proceedings held on
        20 December 2010, with reasons dispatched on 18 January
        2011, refusing European patent application
        No. 09 157 010.1

II.   The decision under appeal was based on a main request
        and four auxiliary requests. The main request was
        refused due to lack of novelty (Article 54 EPC) having
        regard to the document:

        D3: US 5 830 064.

        The first auxiliary request was refused due to lack of
        clarity (Article 84 EPC) and lack of novelty
        (Article 54 EPC) having regard to D3.

        The second and third auxiliary requests were refused
        due to lack of clarity (Article 84 EPC).

        The fourth auxiliary request was refused due to lack of
        clarity (Article 84 EPC) and lack of inventive step
        (Article 56 EPC) having regard to the documents:

        D1: US 2004/0108945 or

        D4: JP 55 133158.

        A fifth auxiliary request filed during oral proceedings
        before the examining division was not admitted under
        Rule 137(3) EPC.

III.   Notice of appeal was received on 28 March 2011. The
       appeal fee was paid on the same day. A statement
       setting out the grounds of appeal was received on
       27 May 2011. The appellant (applicant) requested that
       the decision of the examining division be set aside and
       that a patent be granted on the basis of a main request
       or four auxiliary requests (i.e. first, second, third
       and fourth) submitted with the statement setting out
       the grounds of appeal. The appellant provided arguments
       as to the novelty and inventive step of the requests,
       having regard to the disclosure of the documents D1,
       D3, D4 and documents:

       D2: EP 0 845 779, and

       D5: GB 2 319 938.

       The appellant also re-filed description pages 1, 2, 2a
       and 3 to 6 as well as Figures 1(a) to 1(d), 2 to 4 and
       5(a) to 5(e). In addition, oral proceedings were
       requested as an auxiliary measure.

IV.   A summons to oral proceedings scheduled for 13 June
       2014 was issued on 19 March 2014. In an annex to this
       summons pursuant to Article 15(1) RPBA the board gave
       its preliminary opinion on the appeal. In particular,
       the board indicated that it considered the prior art
       acknowledged by the appellant itself in the description
       (see paragraphs [0002] to [0005] and the corresponding
       Figures 1(a) to 1(d) of the published application) as
       the closest prior art for the subject-matter of the
       claims of the five requests. Objections under
       Article 56 EPC were then raised for all requests in
       view of said prior art and of the disclosure of D2 or
       D4.

V.   With a letter of reply dated 9 May 2014, the appellant
        submitted arguments in support of inventive step,
        together with a sworn statement from one of the
        inventors under Article 117(1)(g) EPC.

VI.   Oral proceedings were held as scheduled on
        13 June 2014. During them, the appellant presented
        further arguments. It requested that the decision under
        appeal be set aside and that a patent be granted on the
        basis of the main request, or of one of the first to
        fourth auxiliary requests, submitted with the statement
        setting out the grounds of appeal. At the end of the
        oral proceedings, the decision of the board was
        announced.

VII.   Claim 1 of the main request reads as follows:

        "A method for converting an analog signal to a digital
        signal encoded to have a digital code (195, 205), the
        method comprising:
        receiving the analog signal;
        measuring a voltage of the analog signal (190) with
        respect to a sampling point;
        selecting, based on the voltage measured, the digital
        code (195, 205) comprising a plurality of binary bits,
        wherein all binary bits of the digital code (195, 205)
        are zero if the measured voltage of the analog signal
        (190) is zero, and wherein all binary bits of the
        digital code (195, 205) change state from zero to one
        when the analog signal crosses zero volts in a negative
        direction;
        inverting substantially one half of the plurality of
        binary bits of the digital code (195, 205) to produce a
        modified digital code (215, 310) to represent the
        analog signal at the sampling point."

The main request comprises further independent claims directed to a corresponding circuit (claim 13) and to a corresponding method (claim 7) and circuit (claim 14) for converting a digital signal to an analog signal.

The subject-matter of the independent claims of the auxiliary requests is not relevant for the decision of the board.

Reasons for the Decision

1.   Admissibility of the appeal

The appeal complies with Articles 106 to 108 EPC (cf. point II above) and is therefore admissible.

2.   Main request - Admissibility

Independent claims 1, 7, 13 and 14 have been amended in substance, with respect to the claims of the main request on which the decision was based, by adding the feature that the digital code which is selected based on the measured voltage of the analog signal is of the type wherein all binary bits are zero if the measured voltage is zero and all binary bits change state from zero to one when the analog signal crosses zero volts in a negative direction.

The added feature is disclosed in paragraphs [0005] and [0006] and in Figures 1(d) and 3 of the published application. Moreover, this amendment was made with the aim of overcoming the novelty objection based on D3, which was the ground for the refusal of the then main

request, since the added feature was not disclosed in
D3.

The board therefore decided to admit the main request
into the appeal proceedings in the exercise of its
discretionary power under Article 12(4) RPBA.

3.   Main request - Novelty and inventive step

3.1   Prior art

D1 discloses a digital encoder acting on an n-bit data
signal; upon receiving n-bit data, the encoder counts
the number of changes, i.e. from "0" to "1" and vice-
versa, in consecutive bits (see Figure 2, counter 12).
If the count is greater than 3, some bits of the data
are inverted (see Figure 2, inverters 31 for bit
numbers 0, 2, 4 and 6). By thus decreasing the number
of the changing points in the n-bit data, high-
frequency components of data and electro-magnetic
interferences are reduced. D1 thus does not disclose
the particular digital coding of an analog signal
around the zero voltage as used in the present
application. Moreover, D1 does not address the problems
caused by a change of the n-bit data from a sequence of
consecutive "0" bits to a sequence of consecutive "1"
bits. Furthermore, when the n-bit data is a consecutive
sequence of "0s" or a consecutive sequence of "1s", the
encoder of D1 does not perform any inversion on the
bits since the counter does not count any changing
point in that case.

D2 discloses a system for receiving a one-bit signal,
grouping the bits in four words of 16-bits each and
inverting one half of the words (see Figure 1).
Therefore D2 does not disclose the particular digital

coding of an analog signal around the zero voltage as
used in the present application. Moreover, even if a
16-bit word could be considered to be a digital code
representing an analog voltage signal, either all the
bits or none of the bits in this word are inverted,
instead of half of the bits in a code-word being
inverted as in the claimed method.

D3 discloses a system for generating a random number
based on the sampling of an analog noise signal.
Sampling the noise signal generates a sequence of
N random bits at each sampling time (see col. 5,
lines 37-40). D3 is however silent about the digital
coding used. D3 teaches to further process the
sequences of N-bits to increase their randomness. This
is performed by inverting selected N-bits sequences.
Either every second N-bits sequence is selected for
inversion or a random mask is used for selection (see
in that respect Figures 2 and 4 provided by the
appellant in the statement setting out the grounds of
appeal). In both cases however, whole N-bits sequences
are inverted and not half of an N-bits code-word as
required by the present application.

D4 discloses a system for converting an analog signal
to a binary signal using a so-called folded binary
code. Tables 1 and 2 of D4 show that a zero voltage
crossing of the analog voltage does not lead to a
change from a sequence of consecutive "0s" to a
sequence of consecutive "1s" in the digital code but
rather leads to a change of only one bit in the
sequence. D2 aims at diminishing long series of "0"
bits in a code-word by inverting n contiguous bits in
an N-bits code-word.

D5 discloses an analog to digital converter without giving any details about the digital code used.

None of documents D1 to D5 deals with the digital coding of an analog signal, wherein all binary bits of the digital code are zero if the analog signal is zero, and wherein all binary bits of the digital code change state from zero to one when the analog signal crosses zero in a negative direction, as required by the claims. Moreover the technical problem, as stated in the description (see paragraph [0006] of the published application), is the direct consequence of this precise feature of the digital code used.

Therefore the board judges that the prior art acknowledged by the appellant itself in the description in paragraphs [0002] to [0005] and the corresponding Figures 1(a) to 1(d) of the published application represents a much more suitable starting point for the assessment of inventive step of the claims and represents the closest prior art. The digital coding represented on Figure 1(d) is well-known in the art and usually referred to as the "2's complement coding".

3.2   The subject-matter of claim 1 differs from this prior art by the step of inverting substantially one half of the plurality of binary bits of the digital code to produce a modified digital code to represent the analog signal at the sampling point.

The technical effect of this distinguishing feature is that existing code-words in the look-up table containing long sequences of consecutive "0" bits or long series of consecutive "1" bits are suppressed, while new code-words containing long series of "0" bits or "1" bits may be inserted into the look-up table. In

particular, it is apparent that the two code-words coding the zero voltage value and its adjacent negative voltage value are no longer a series of only "0" bits and only "1" bits, respectively. Therefore, in the case of an analog voltage centred at zero volts and changing around this value, the change in code-words does not imply a change of all binary bits in the same direction at the same time on the parallel outputs of the A/D converter. The noise induced by the alternation of all ones and zeros on the parallel output bus of the A/D converter is thus reduced in that case with respect to the voltage value itself.

The presence of noise in an A/D converter at very low analog input power and zero crossing was known at the priority date of the application as the "digital feedback problem", as plausibly argued by the appellant at the oral proceedings and in the letter of 27 May 2014 with reference to the content of the sworn statement from one of the inventors, submitted as annex to the letter of 27 May 2014.

The objective technical problem may thus be defined as how to reduce the digital feedback in the prior art A/D converter. In that respect, the board agrees with the appellant that introducing the digital coding itself as being the cause of digital feedback in the formulation of the problem would introduce an inadmissible pointer to the solution.

As is apparent from paragraph 3.1, the skilled person does not get any hint from prior-art documents D1 to D5 to solve this problem since none of these documents is concerned with the noise induced at low analog voltage in an A/D converter. The appellant put forward the convincing argument that the skilled person would

rather use one of the known options at its disposal, such as the Gray coding, the folded binary coding, a randomisation technique or the injection of an offset voltage. None of these prior-art methods is based on the use of a 2's complement coding around the zero value and the inversion of half of the bits of the code words, as defined in claim 1. The solution proposed by claim 1 can thus be seen as a non-obvious alternative to the above-mentioned known solutions.

For these reasons, the board judges that the subject-matter of claim 1 involves an inventive step (Article 56 EPC), having regard to the cited prior art.

The further independent claims are directed to a corresponding circuit (claim 13) and to a corresponding method (claim 7) and circuit (claim 14) for converting the digital signal provided by the method of claim 1 back to an analog signal. Therefore independent claims 7, 13 and 14 also meet the requirements of Article 56 EPC.

4.   In conclusion, the main request is allowable. There is thus no need for the board to examine the first to fourth auxiliary requests.

Order

For these reasons it is decided that:

1.   The decision under appeal is set aside.

2.   The case is remitted to the department of first
        instance with the order to grant a patent on the basis
        of claims 1 to 14 of the main request, description
        pages 1, 2, 2a and 3 to 6 and figures 1(a) to 1(d), 2,
        3, 4, 5(a) to 5(e), as submitted with the statement
        setting out the grounds of appeal.

The Registrar: The Chair:

G. Nachtigall   A. Ritzka

Decision electronically authenticated