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Case Number: T 1345/11 - 3.5.06

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Language of the proceedings: EN

Title of invention:
Integrated circuit I/O using a high performance bus interface

Patent Proprietor:
Rambus Inc.

Former Opponent:
MICRON EUROPE Ltd
MICRON Semiconductor Deutschland GmbH
SK hynix Deutschland GmbH
Infineon Technologies AG

Headword:
DRAM/RAMBUS 2

Relevant legal provisions:
EPC 1973 Art. 100(c)

Keyword:
Grounds for opposition - extension of subject-matter (yes)

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T 0331/87

Catchword:

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Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 1345/11 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 29 June 2016

Appellant: (Patent Proprietor)	Rambus Inc. 1050 Enterprise Way, Suite 700 Sunnyvale, CA 94089 (US)
Representative:	Eisenführ Speiser Patentanwälte Rechtsanwälte PartGmbB Johannes-Brahms-Platz 1 20355 Hamburg (DE)
Respondent: (Former Opponent 1)	MICRON EUROPE Ltd Micron House Wellington Business Park Dukes Ride Crowthorne Berkshire RG45 6LS (GB)
Representative:	Tunstall, Christopher Stephen Carpmaels & Ransford LLP One Southampton Row London WC1B 5HA (GB)
Respondent: (Former Opponent 2)	MICRON Semiconductor Deutschland GmbH Sternstr. 20 85609 Aschheim (DE)
Representative:	Lang, Johannes Bardehle Pagenberg Partnerschaft mbB Patentanwälte, Rechtsanwälte Postfach 86 06 20 81633 München (DE)
Respondent: (Opponent 3)	SK hynix Deutschland GmbH Am Prime Parc 13 65479 Raunheim (DE)

Representative:	Ter Meer Steinmeister & Partner Patentanwälte mbB Nymphenburger Straße 4 80335 München (DE)
Respondent: (Former Opponent 4)	Infineon Technologies AG St.-Martin-Strasse 53 81669 München (DE)
Representative:	Hess, Peter K. G. Bardehle Pagenberg Partnerschaft mbB Patentanwälte, Rechtsanwälte Postfach 86 06 20 81633 München (DE)
Decision under appeal:	**Decision of the Opposition Division of the European Patent Office posted on 20 May 2011 revoking European patent No. 1022642 pursuant to Article 101(3)(b) EPC.**

Composition of the Board:

Chairman	W. Sekretaruk
Members:	A. Teale
	M. Müller

Summary of Facts and Submissions

I. This is an appeal by the patent proprietor, the sole appellant in these proceedings, against the decision by the opposition division, dispatched with reasons on 20 May 2011, to revoke European patent No. 1 022 642.

II. The patent derives from a second generation divisional application from a grandparent application which has been referred to in these proceedings as the "PCT application" (also as "U1" and "GPA"). More specifically, the patent results from European patent application No. 00108822.8, a divisional application of European patent application No. 99118308.8, which was itself a divisional application of European patent application No. 91908374.1, filed as International patent application No. PCT/US91/02590, the "PCT application", which was published as WO 91/16680 A1.

III. Claims 103 and 104 of the PCT application read as follows (emphasis by the board):

"103. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, **and has substantially fewer bus lines than the number of bits in a single address**, said semiconductor device comprising connection means adapted to connect said semiconductor device to said bus, and at least one modifiable access-time register accessible to said bus through said connection means, whereby data may be

transmitted to said register via said bus which establishes a predetermined amount of time that said semiconductor device thereafter must wait before using said bus in response to a request."

"104. The semiconductor device of claim 103 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus."

IV. Four oppositions were received against the granted patent from opponents 1 to 4, later respondent opponents 1 to 4, respectively. Taken together, the four oppositions were based on the grounds of opposition foreseen in Article 100(a) (novelty and inventive step), (b) and (c) EPC 1973 (extension beyond the content of the application as filed and of the earlier application as filed, namely the PCT application).

V. During opposition proceedings, in a letter received on 23 March 2005, opponent 4 withdrew its opposition.

VI. The reasons for the appealed decision stated *inter alia* that claim 1 of the main request (maintenance of the patent as granted, rejection of the oppositions) and auxiliary requests I to VI (relating to amended patent claims) contained subject-matter both through the addition of features ("d" to "h" relating to output drivers and rising and falling edge transitions) and through the deletion of features ("M0" to "M2" relating to the bus) extending beyond the content of the PCT application, Articles 100(c) and 76(1) EPC. Claim 1 according to auxiliary requests VII to XVIII (also relating to amended patent claims) was found to contain

subject-matter through the addition of features ("d" to "h" relating to output drivers and rising and falling edge transitions) extending beyond the content of the PCT application, Article 76(1) EPC.

VII. A notice of appeal was received from the proprietor on 15 June 2011, requesting that the decision be set aside and that the patent be maintained as granted. An auxiliary request was also made for oral proceedings. The appeal fee was paid on the same day.

VIII. With a statement of grounds of appeal, received on 28 September 2011, the appellant proprietor refiled auxiliary requests I to XVIII, upon which the appealed decision was based, and requested that the oppositions be rejected (main request) or that the decision be set aside and that the patent be maintained in amended form according to one of auxiliary requests I to XVIII.

IX. In a submission received on 14 February 2012 respondent opponent 3 argued *inter alia*, relying on Article 100(c) EPC, that the subject-matter of the patent according to the appellant proprietor's main and eighteen auxiliary requests extended beyond the content of the PCT application as filed in view of the features in claim 1 added with respect to claim 103 of the PCT application, namely "d" to "h" (relating to output drivers and rising and falling edge transitions) and the deleted features "M0" to "M2" (relating to the bus).

X. On 22 February 2012 a response to the appeal was received from respondent opponent 1.

XI. In a letter received on 12 July 2013 respondent opponent 3 withdrew its opposition.

XII. In a letter received on 30 January 2014 respondent opponent 2 withdrew its opposition.

XIII. In a letter received on 4 February 2014 respondent opponent 1 withdrew its opposition.

XIV. In a letter received on 8 March 2016 the appellant proprietor withdrew its request for oral proceedings and stated that "The patent proprietor does not intend to amend its case any further and rather requests a decision in accordance with the present status of the file."

XV. Claim 1 according to the appellant proprietor's main request (the patent as granted) reads as follows:

"A synchronous semiconductor memory device having at least one memory array (1) which includes a plurality of memory cells, the memory device comprising: clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54) having a fixed frequency; a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal (53, 54) to transpire after which the memory device responds to a read request; and a plurality of output drivers (76) for outputting data in response to the read request, the output drivers (76) outputting a first portion of data synchronously with respect to a rising edge transition of the external clock signal (53, 54) and the output drivers (76) outputting a second portion of data synchronously with respect to a falling edge transition of the external clock signal (53,54), wherein the first and second portions of data are output after the number of clock cycles of the external clock signal (53, 54) transpire, and wherein both the rising edge transition

of the external clock signal and the falling edge transition of the external clock signal both transpire in the same clock period of the external clock signal (53, 54)."

XVI. Claim 1 according to the auxiliary requests I to XVIII can be split into four groups, namely I to V, VI to IX, X to XIII and XIV to XVIII. Taking the first group (I to V), claim 1 according to auxiliary request I only differs from that according to the main request in editorial amendments. Claim 1 according to auxiliary request II differs from that according to auxiliary request I in the restriction of the memory device to a "Dynamic Random Access Memory (DRAM)" memory device, the restriction to the plurality of memory cells being "arranged in rows and columns", the restriction of the read request to being "received synchronously with respect to the external clocks signal", the addition of the feature "wherein the output drivers (76) output the data after the number of clock cycles of the external clock signal transpire and synchronously with respect to the external clock signal (53, 54) so that the read request and the corresponding response are separated by the number of clock cycles as selected by the value stored in the programmable access-time register", the deletion of the expression "wherein the first and second portions of data are output after the number of clock cycles of the external clock signal (53, 54) transpire" and the addition at the end of the expression "so that each output driver of the plurality of output drivers (76) outputs data at a bus cycle data rate that is twice the rate of the external clock signal".

XVII. Auxiliary requests III, VII, XI and XV all have the effect of adding the following passage at the end of

claim 1 "and clock generation circuitry (101, 111), coupled to the clock receiver circuitry, to generate an internal clock signal (73), and wherein the plurality of output drivers (76) output data in response to the internal clock signal (73)". Auxiliary requests IV, VIII, XII and XVI all have the effect of adding the passages to claim 1 "wherein the value is further representative of a second number of clock cycles of the external clock signal after which the DRAM responds to a write request by receiving write data to be stored in the DRAM, wherein the write request is received synchronously with respect to the external clock signal" and "a plurality of input receivers to receive the write data from the external bus in response to the write request, wherein the input receivers input the data from the external bus after the second number of clock cycles transpire so that the write request and the corresponding receipt of write data are separated by the second number of clock cycles as selected by the value stored in the programmable access-time register" and the amendment of "number" to "first number". Auxiliary requests V, IX, XIII and XVII all have the effect of adding the passage to claim 1 "wherein the clock generation circuitry includes a delay locked loop coupled to the clock receiver circuitry (101, 111) to generate the internal clock signal (73)". Auxiliary request V also adds the passage to claim 1 "wherein data is transmitted to the programmable access-time register to set the value in the programmable access-time register".

XVIII. Regarding the second group of auxiliary requests (VI to IX), claim 1 of these requests is based on that of auxiliary request II with the addition of the expressions "the DRAM being capable of use in a semiconductor bus architecture including a plurality of

semiconductor devices connected in parallel to a bus, wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said DRAM for communication with substantially every other semiconductor device connected to said bus, **and has substantially fewer bus lines than the number of bits in a single address**" (emphasis by the board) and "wherein data is transmitted to the programmable access-time register to set the value in the programmable access-time register".

XIX. Turning to the third group of auxiliary requests (X to XIII), claim 1 according these requests differs from that according to auxiliary request II in the addition of the passages "connection means adapted to connect the DRAM to an external bus which is part of a semiconductor bus architecture, the semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, and wherein the bus uses **address multiplexing** to convey a single memory address" (emphasis by the board) and "the programmable access-time register being accessible to the external bus through the connection means, wherein data is transmitted to the programmable access-time register over the external bus to set the value in the programmable access-time register" and the expressions "onto the external bus" and "on the external bus".

XX. Taking the fourth group of auxiliary requests (XIV to XVIII), claim 1 of these requests differs from that of

auxiliary request II in the addition of the passages "connection means adapted to connect the DRAM to an external bus which is part of a semiconductor bus architecture, the semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, **and wherein the external bus has substantially fewer bus lines than the number of bits in a single address**" (emphasis by the board) and "the programmable access-time register being accessible to the external bus through the connection means, wherein data is transmitted to the programmable access-time register over the external bus to set the value in the programmable access-time register" and the expressions "onto the external bus" and "on the external bus". Claim 1 of auxiliary request XVIII differs from that of auxiliary request XVII in the addition at the end of a passage relating to a plurality of sense amplifiers.

Reasons for the Decision

1. The admissibility of the appeal

The appeal fulfills the admissibility criteria under the EPC and is consequently admissible.

2. The technical context of the invention

The present invention concerns a dynamic random access memory (DRAM) semiconductor device having at least one

memory array which includes a plurality of memory cells arranged in rows and columns; see figure 1. The DRAM contains connection means for connecting it to an external bus which is a part of a semiconductor bus architecture comprising a plurality of semiconductor devices connected in parallel to the external bus; see figure 2. The external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus. Said connection means comprise a plurality of input receivers (71, 72) to receive data from the external bus and a plurality of output drivers (76) for outputting data to the external bus; see figure 10. The device further comprises a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal to transpire after which the DRAM responds to a read request.

3. The ground of opposition under Article 100(c) EPC 1973

3.1 According to the appealed decision, the patent according to the main request, i.e. the patent as granted, extended beyond the content of the PCT application as filed, so that the ground of opposition under Article 100(c) EPC prejudiced the maintenance of the patent. Regarding the auxiliary requests, the amended patent was found not to meet the requirements of Articles 100(c) and 76(1) EPC because the amended patent extended beyond the content of the PCT application as filed, Article 101(3)(b) EPC.

3.2 Since the filing date of the patent (16 April 1991) lies before the entry into force of EPC 2000 on

13 December 2007, Article 100(c) EPC 1973 is applicable to the present case. Moreover, since the patent had already been granted at the time of entry into force of EPC 2000, the decision to grant being dated 26 July 2001, Article 101 EPC also applies to the present case.

3.3 According to Article 101(2) EPC, if the opposition division is of the opinion that at least one ground for opposition prejudices maintenance of the European patent, it shall revoke the patent. This applies both to the patent as granted (main request) and to the amended patent (auxiliary requests). One of the grounds for opposition relied upon by the respondent opponents is that set out in Article 100(c) EPC 1973, namely that the subject-matter of the European patent extends beyond the content of the earlier application as filed. In the present case the parties, the opposition division and the board all understand the expression "earlier application" as referring to the PCT application.

4. The appellant proprietor's main request

4.1 According to the reasons for the appealed decision (see point 5.3), *inter alia* the feature (M2) that "[the bus] has substantially fewer bus lines than the number of bits in a single address", which was present in independent claim 103 of the PCT application, is not present in claim 1 of the main request. The proprietor argued that this feature was standard at the priority date and, anyway, it was contradicted by page 8, lines 4 to 7, of the PCT application which stated that "16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention", suggesting that the number of bus lines was immaterial.

In its decision the opposition division found that deleting this feature had caused the subject-matter of the patent to extend beyond the content of the earlier application as filed.

4.2 In the grounds of appeal the appellant proprietor argued *inter alia* (see section III.2, pages 29 to 39) that granted claim 1 was based on claim 103 of the PCT application which set out a semiconductor device rather than a bus or a semiconductor bus architecture. The fact that the claimed semiconductor device could be used in such an architecture did not mean that it had to be connectable to all the bus lines of the "inventive bus" embodiment disclosed in the PCT application and summarized in the "Summary of Invention" on page 7, lines 9 to 19. In the light of claim 104, which stated that the semiconductor device "connects substantially only to said bus", claim 103 could be understood to cover further connection means to further bus and non-bus lines, figure 2 showing two non-bus lines, namely the chained "ResetIn/ResetOut" line. The feature that the bus has substantially fewer bus lines than the number of bits in a single address had to be understood in the sense of address multiplexing, for instance splitting cell addresses into a row address and a column address, stated in the description to be a conventional approach to reducing the number of pins needed to transmit the address; see page 2, line 23, to page 3, line 3. Address multiplexing *per se* could not be considered to be inventive, and the skilled person would have realized that a "narrow bus" was not an element of the invention. Hence the features of the semiconductor device set out by claim 103 actually reduced to connection means for connecting the device to a conventional address-multiplexed bus and the features

of the at least one modifiable access-time register. Even if the deletion of the bus features from claim 1 resulted in a generalisation, the amendment fulfilled the criteria set out in T 0331/87 (OJ EPO 1991, 022).

4.3 The respondent opponents have argued *inter alia* that the subject-matter of the patent according to the appellant proprietor's main and auxiliary requests extended beyond the content of the PCT application as filed in view of the deleted bus features "M0" to "M2".

4.4 The disclosure in the PCT application

4.4.1 The bus

According to the summary of the invention in the PCT application, the bus "includes clock signals, power and multiplexed address, data and control signals"; see page 8, lines 1 to 2. The description then gives an example of the bus, which the board understands to be illustrated in figure 2 (see, in particular, lines BUSDATA[0]-[7], CLOCK1, CLOCK2, GND, V_{DD}): "In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide". The section entitled "Bus" also concerns eight multiplexed bus lines (BusData[0:7]) carrying address, data and control signals; see page 18, line 21, to page 19, line 21. The board understands this disclosure to mean that the address, data and control signals are all carried by the same multiplexed bus lines, albeit at different times. The bus has substantially fewer bus lines than the number of bits in a single address (see page 7, lines 16 to 17) because an address word is split into several parts (see figure 4) before being sent over the multiplexed bus lines and then

reassembled, a technique acknowledged as prior art in the description; see page 2, line 23, to page 3, line 3. In the light of this disclosure, the board does not accept the appellant proprietor's argument that the "bus" can be considered to be only those lines carrying parts of address words, since the bus is disclosed as not only comprising multiplexed address, data and control signals, but also clock signals and power lines, as illustrated in figure 2; see the lines CLOCK1, CLOCK2, GND and V_{DD}. The fact that the bus disclosed in the PCT application uses address multiplexing, a technique acknowledged as being conventional in the description, does not necessarily mean that the skilled person would have understood address multiplexing to be optional. Moreover the feature that the bus has substantially fewer bus lines than the number of bits in a single address is not understood as a synonym for a bus using address multiplexing, since the description makes clear that the bus is also used to carry data and control signals; see page 8, lines 1 to 2. Address multiplexing implies a limitation of the number of device address pins but not a limitation on the number of data and control pins. Hence a device having address multiplexing may connect to a bus having few multiplexed bus lines but an unspecified number of data and control lines, so that the entire bus to which it is adapted to connect need not have substantially fewer bus lines than the number of bits in a single address. Hence, as the opposition division put it, the feature of "address multiplexing" is broader than the feature that "the bus has substantially fewer bus lines than the number of bits in a single address".

4.4.2 The multiple-bus embodiments

Figure 3 illustrates three DRAM devices 15, 16, 17 having pins on one side, the pins being connected directly to the "primary" bus 18; see page 10, line 12. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20; see page 9, lines 19 to 22. Figure 9 shows an embodiment with a higher level of integration where several "subsystems", each comprising DRAM devices (15, 16, 17), a primary bus (18) and a transceiver (19), are all connected via their respective transceiver to a "transceiver bus" (65): see page 49, lines 8 to 12. The board finds it significant that, although multiple-bus arrangements comprising a plurality of said subsystems are discussed, the connection to the DRAM devices themselves remains in every case the "primary bus".

4.4.3 The semiconductor device interface

Claim 1 of the patent and claim 103 of the PCT application refer to "connection means". The board understands these in the context of the "device interface" disclosed from page 53, line 4, to page 59, line 2, of the PCT application. The device interface comprises the electrical interface comprising input receivers, bus drivers and clock generation circuitry. The board understands from this that the features of the connection means reflect the features of the primary bus, in particular the functions of the various bus lines. In other words, contrary to the argument by the appellant proprietor, the features of the bus do imply a restriction of the features of the DRAM device to at least be adapted to the narrow bus mentioned in original claim 103. As disclosed in original claims (or "embodiments") 82 and 92, the connecting means consists

of pins for connection to the external bus and corresponding wires for connection with the internal bus logic. The adaptation of the semiconductor device for connection to the narrow bus does not limit the number of pins that the semiconductor device has, as there may be unused pins just as there may be unused bus lines. However, the number of pins carrying bus signals is determined by the internal bus logic. Thus the "narrow bus" feature in combination with the connecting means adapted to it implies that the claimed semiconductor device "has substantially fewer" pins carrying bus signals "than the number of bits in a single address".

4.5 The amendments to claim 1 of the main request

4.5.1 The board agrees with the parties that claim 103 of the PCT application forms the basis for claim 1 of the present main request, various features having been either added or deleted. In particular, the feature that the bus "has substantially fewer bus lines than the number of bits in a single address" (the "narrow bus" feature "M2") has been deleted.

4.5.2 The appellant proprietor has argued that claims 103 and 104 and the description of the PCT application provide a basis for this amendment. The board disagrees. All of the independent claims in the PCT application setting out a bus, including claim 103, contain the feature that the bus has "substantially fewer bus lines than the number of bits in a single address". This is consistent with the example given on page 8, lines 2 to 4, of memory addresses being up to 40 bits wide but the bus having only twelve lines (see figure 2), namely clock lines CLOCK1 and CLOCK2, power lines V_{DD} and GND,

and multiplexed address, data and control signals BUSDATA[0]-[7].

4.5.3 Consequently the board finds that the subject-matter of claim 1 according to the main request (the granted patent) extends beyond the content of the earlier application as filed. Hence Article 100(c) EPC 1973 prejudices maintenance of the patent as granted, Article 101(2) EPC.

4.5.4 The same applies to claim 1 according to auxiliary request I (containing only editorial amendments with respect to claim 1 as granted) so that Article 100(c) EPC 1973 prejudices maintenance of the patent according to auxiliary request I, Article 101(2) EPC.

5. The appellant proprietor's auxiliary requests II to V

Like claim 1 of the main request, claim 1 of these auxiliary requests does not set out the feature that the bus "has substantially fewer bus lines than the number of bits in a single address" (the "narrow bus" feature "M2"). Hence, for the same reasons as given for the main request, Article 100(c) EPC 1973 prejudices maintenance of the patent according to auxiliary requests II to V, Article 101(2) EPC.

6. The appellant proprietor's auxiliary requests X to XIII

6.1 Like claim 1 of the main request, claim 1 of these auxiliary requests does not set out the feature that the bus "has substantially fewer bus lines than the number of bits in a single address" (the "narrow bus" feature "M2"), but does instead set out the feature that "the bus uses address multiplexing to convey a single memory address" (the "address multiplexing" (AM)

feature referred to by the respondent opponents). The appellant proprietor has argued that the two features have the same meaning. As stated above (see point 4.4.1), the board disagrees, finding the feature of "address multiplexing" to be broader than the feature that "the bus has substantially fewer bus lines than the number of bits in a single address". As stated above, address multiplexing implies a limitation of the number of device address pins but not a limitation on the number of data and control pins. Hence the replacement of the "narrow bus" feature by the address multiplexing feature causes claim 1 of these requests to cover bus configurations that were not directly and unambiguously derivable from the PCT application as originally filed.

6.2 Claim 104 of the PCT application, which sets out the device connecting substantially only to said bus and sending and receiving substantially all address, data and control information over said bus, restricts the features of the device rather than those of the bus itself. For this reason the board does not accept the appellant proprietor's argument that, in the light of claim 104, claim 103 can be understood as disclosing a more general bus having fewer lines. Hence the arguments based on claim 104 do not change the analysis, set out above, of claim 1 of these requests.

6.3 Hence the subject-matter of claim 1 of these auxiliary requests extends beyond the content of the earlier application as filed and Article 100(c) EPC 1973 prejudices maintenance of the patent according to auxiliary requests X to XIII, Article 101(2) EPC.

7. The appellant proprietor's auxiliary requests VI to IX and XIV to XVIII

7.1 Claim 1 of these requests sets out the features (referred to as M0 to M2 in the appealed decision) of the bus defined in claim 103 of the PCT application including the feature (M2) that the bus "has substantially fewer bus lines than the number of bits in a single address". For this reason it overcomes the objections raised above against the previous requests.

7.2 According to the reasons for the appealed decision (section 5.2), the following features, which are not present in claim 103 of the PCT application but were set out in claim 1 according to *inter alia* auxiliary requests VI to IX and XIV to XVIII, set out an impermissible intermediate generalisation relating to the operation of output drivers in relation to a clock signal and thus comprise subject-matter extending beyond the content of the PCT application as originally filed:

d. a plurality of output drivers for outputting data in response to the read request;

e. the output drivers outputting a first portion of data synchronously with respect to a rising edge transition of the external clock signal;

f. the output drivers outputting a second portion of data synchronously with respect to a falling edge transition of the external clock signal,

g. wherein the first and second portions of data are output after the number of clock cycles of the external clock signal transpire,

h. wherein both the rising edge transition of the external clock signal and the falling edge transition of the external clock signal both transpire in the same clock period of the external clock signal.

According to the decision, the description of the PCT application discloses the operation of the output drivers in relation to a clock signal, in particular in figure 10 and the corresponding text from page 53, line 23, onwards. In this embodiment, the operation of the output drivers is only described in combination with two features, namely (feature I) the use of true and complement internal device clocks to select which data is driven to the output drivers (see page 58, lines 21 to 23) and (feature II) the output of data with respect to an internal clock derived from early and late bus clocks; see figure 8, page 46, line 19, to page 48, line 17, page 53, section "Electrical Interface - Input/Output Circuitry" and page 56, line 21, to page 57, line 2. Regarding feature I, no other way was disclosed of outputting data twice per internal clock cycle other than using the true and complement internal device clocks to select which data was driven to the output drivers. Regarding feature II, in view of figure 8 and the accompanying text, a given device never saw a single "external clock signal", but only early and late bus clocks. The board comments on the meaning of "internal" and "external" clocks below.

Consequently, so the decision, by setting out features (d) to (h), but not features I and II, the claims set out an impermissible intermediate generalisation between the detailed disclosure of the description of the PCT application and that of claim 103.

7.3 The appellant proprietor has denied that an impermissible intermediate generalisation has occurred (see grounds of appeal, pages 10 to 28), since the features referred to in the decision were not inextricably linked. According to claim 103 of the PCT application, the modifiable access-time register established a predetermined amount of time that the semiconductor device thereafter must wait before using the bus in response to a request. A skilled person would understand that operation of the semiconductor device was synchronised to a clock, the "predetermined amount of time" being expressed as a number of clock cycles. The PCT application also disclosed (see page 48, lines 6 to 17) the option of output drivers outputting data synchronously with respect to both a rising and a falling edge transition of the external clock signal, as set out in features "e" and "f" above; see "Thema I" in the grounds of appeal. The bus/device clock rate (250 MHz) was equal to the bus cycle data rate (500 MHz) divided by two. The skilled person would understand this to mean that two bits per bus/device clock cycle had to be output, which meant that data had to be output on both rising and falling edges of the bus/device clock. Such an exemplary embodiment was disclosed in the section "Electrical Interface - Input/ Output Circuitry" of the PCT application, setting out a preferred input/output circuit operable at high clock rates; see page 53, line 23, to page 59, line 2, and figure 13. In this embodiment an internal clock signal (73), synchronized with the external clock signal (bus clock 1/2), is produced together with its complement (74). Without the exemplary embodiment, the skilled person had only the disclosure on page 48, lines 6 to 10, claim 103 of the PCT application not being limited to high clock rates. Outputting data synchronously with

rising and falling edge transitions of the external clock, as set out in the claims, implied an internal clock synchronized with the external clock. The exemplary embodiment went beyond this in achieving a data rate equal to twice the clock rate by dividing each clock cycle into an even bus cycle and an odd bus cycle, the falling and rising edges distinguishing the even from the odd cycles; see page 19, lines 15 to 17, of the PCT application. There was no intermediate generalisation because the concepts of producing an internal clock and outputting data on both clock edges were not disclosed as being inextricably linked. The appellant proprietor also disputed the statement in the decision that no other way was disclosed of outputting data twice per internal clock cycle than that of true and complement internal clocks being used to select which data was driven to the output drivers. The skilled person would have understood that other ways were possible. The appellant proprietor also disputed the statement in the decision that it was not derivable from the PCT application that data driven to the output drivers could be selected by rising or falling edges of a single clock signal. Both the true and complement clock signals contained all the information required to operate the output multiplexer shown in figure 10, so that either one alone would suffice.

7.4 The PCT application also disclosed the further option, particularly important in high-clock-rate systems, of using a clock spreading scheme with early and late bus clocks to derive synchronised clock signals in the various chips of a bus architecture in spite of clock propagation delays; see "Thema II" in the grounds of appeal and the section in the PCT application entitled "clocking"; see page 46, line 19, to page 48, line 17. Figure 8a and 8b illustrated a preferred embodiment in

which the edges of the early and late clocks, derived from the same clock but differently routed, are compared to cancel out propagation delays and derive a unique synchronized clock for all devices; see figure 8b; 59, 60. The clock spreading scheme was only necessary when using a high clock rate.

7.5 Respondent opponent 3 has argued (see pages 49 to 51 of the submission of 14 February 2012) that features I and II are presented in the PCT application as being important and inextricably linked with the bus features. Moreover page 1, lines 10 to 13, concerning the field of the invention, referred to "high speed transfer of blocks of data". Page 18, lines 22 to 23, referred to the preferred bus architecture of the invention comprising *inter alia* two clock signals Clk1 and Clk2; see also figure 2. According to page 19, lines 9 to 10, "The two clocks together provide a synchronized, high speed clock for all the devices on the bus". Moreover claim 108 of the PCT application referred to bus features and an internal device clock generating means and early and late bus clock signals. Similar arguments were made by respondent opponent 1; see section III.2, pages 38 to 41, of the submission of 22 February 2012.

7.6 Regarding the terminology used in the claims and description of the PCT application and the present patent, the board notes that the expression "internal" clock is used to distinguish clocks derived within the device (see true clock 73 in figure 12 and true/ complement clocks 73/74 in figure 10) from the "external" clock(s) which the memory device receives from the bus; see early and late external clocks CLOCK1/CLOCK2 in figures 2 and 8a and 53/54 in figure 12. In the context of claim 1 according to auxiliary

requests VI to IX and XIV to XVIII, which mention the rising and falling edge transitions of the "external clock signal", the board understands the expression "external clock signal", in the light of page 58, lines 18 to 23, to mean the "internal device clock"/"true clock" signal 73 derived from the early and late external clock signals; see page 58, lines 1 to 6.

7.7 The question of whether the subject-matter of the amended patent according to these requests extends beyond the content of the earlier application as filed, Article 100(c) EPC 1973, rests on whether it would have been directly and unambiguously derivable for the skilled person from the PCT application that features "I" and "II", set out above, were both merely optional in the context of the output drivers outputting first and second portions of data synchronously with respect to rising and falling edge transitions, respectively, of the external clock signal (features "e" and "f" in the decision).

7.8 The only relevant disclosure of output drivers outputting data synchronously with respect to rising and falling edge transitions of the external clock signal occurs in connection with the derivation of true and complement internal clocks on page 58, lines 18 to 23. This passage states that "The complement internal device clock is used to clock the 'even' input receivers to sample at time 127, while the true internal device clock is used to clock the 'odd' input receivers to sample at time 125. **The true and complement internal device clocks are also used to select which data is driven to the output drivers**" (emphasis by the board.) The derivation of the true and complement internal clocks from an early and a late external clock is set out from page 57, line 3, to

page 58, line 16. Hence the skilled person would understand that the generation of true and complement clocks (feature I above) is disclosed as being a necessary and non-optional precursor to the output drivers outputting first and second portions of data synchronously with respect to rising and falling edge transitions, respectively, of the external clock signal (features "e" and "f" in the decision). The generation of said true and complement internal clocks is disclosed in turn as being based on early and late bus clocks. Hence feature II is disclosed as being a necessary and non-optional precursor to feature I.

7.9 Thus, by setting out features "e" and "f" but not I and II, claim 1 of these requests sets out an impermissible intermediate generalisation, or, put another way, adds subject-matter in the form of the suggestion that features I and II are merely optional, causing the content of the amended patent to extend beyond the content of the PCT application. Hence Article 100(c) EPC 1973 prejudices maintenance of the patent according to auxiliary requests VI to IX and XIV to XVIII, Article 101(2) EPC.

7.10 It follows that none of the appellant proprietor's substantive requests is allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

B. Atienza Vivancos W. Sekretaruk

Decision electronically authenticated