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Datasheet for the decision of 24 June 2015

Case Number: T 1236/11 - 3.5.07

Application Number: 02012810.4

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Language of the proceedings: EN

Title of invention:
Protocol for communication with dynamic memory

Applicant:
Rambus Inc.

Headword:
Communication protocol/RAMBUS

Relevant legal provisions:
EPC Art. 76(1)

Keyword:
Divisional application - subject-matter extends beyond content of earlier application (yes)

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Catchword:

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Case Number: T 1236/11 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 24 June 2015

Appellant: (Applicant)	Rambus Inc. 1050 Enterprise Way, Suite 700 Sunnyvale, CA 94089 (US)
Representative:	Eisenführ Speiser Patentanwälte Rechtsanwälte PartGmbB Johannes-Brahms-Platz 1 20355 Hamburg (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 17 December 2010 refusing European patent application No. 02012810.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	R. Moufang
Members:	R. de Man
	M. Rognoni

Summary of Facts and Submissions

I. The applicant (appellant) appealed against the decision of the Examining Division refusing European patent application No. 02012810.4.

II. The application is a divisional application of European patent application No. 96936776.2, published as WO 97/14289 (the parent application). The Examining Division decided that the subject-matter of the independent claims of a main request, filed with a letter of 8 April 2008, and of auxiliary requests I to IV, filed with a letter of 8 October 2010, extended beyond the content of the parent application as originally filed (Article 76(1) EPC).

III. In the notice of appeal, the appellant maintained the main request and auxiliary requests I to IV and requested oral proceedings on an auxiliary basis.

IV. In a communication accompanying a summons to oral proceedings, the Board expressed the preliminary view that none of the appellant's substantive requests complied with Article 76(1) EPC.

V. With a letter dated 11 May 2015, the appellant withdrew the request for oral proceedings. It stated that it intended neither to attend any oral proceedings nor to amend its case in any respect, and it requested a decision on the state of the file.

VI. Oral proceedings were held on 24 June 2015 in the absence of the appellant. At the end of the proceedings, the chairman pronounced the Board's decision.

VII. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims of the main request or, in the alternative, on the basis of the claims of one of auxiliary requests I to IV.

VIII. Claim 1 of the main request reads as follows:

"A method of operation of a semiconductor memory device (603) that receives an external clock signal, wherein the memory device (603) includes a plurality of banks (602, 606), wherein each bank of the plurality of banks (602, 606) includes a memory cell array, wherein the method comprises:

receiving a first code, wherein the first code indicates that a write operation is to be performed in the memory device (603);

characterized by

sampling the data in response to receiving an external strobe signal, wherein first and second data values of the data are sampled, in succession, during a clock cycle of the external clock signal;

receiving bank selection information, wherein the bank selection information identifies a bank of the plurality of banks (602, 606); and

writing the first and second data values to the memory cell array included in the bank identified by the bank selection information, wherein the first and second data values are written during the write operation."

IX. Claim 1 of auxiliary request I differs from claim 1 of the main request in that the following text is inserted after the passage "sampling the data ... clock signal;":

"wherein the external strobe signal indicates the start of a data transfer;"

X. Claim 1 of auxiliary request II differs from claim 1 of auxiliary request I in that the following text is inserted after the passage "wherein the external ... data transfer;":

"wherein each clock cycle has even and odd phases, wherein the first data value is sampled during the even phase and wherein the second data value is sampled during the odd phase;"

XI. Claim 1 of auxiliary request III reads as follows:

"A method of operation of a semiconductor memory device (603) that receives an external clock signal, wherein the memory device (603) includes a plurality of banks (602, 606), wherein each bank of the plurality of banks (602, 606) includes a memory cell array, wherein the method comprises:

receiving command information including receiving a first code, wherein the first code indicates that one of a read and a write operation is to be performed in the memory device (603);

characterized by

when the first code indicates a write operation, sampling the data in response to receiving an external strobe signal, wherein first and second data values of the data are sampled, in succession, during a clock cycle of the external clock signal; wherein the external strobe signal indicates the start of a data transfer; wherein each clock cycle has even and odd phases, wherein the first data value is sampled during the even phase and wherein the second data value is sampled during the odd phase; and when the first code

indicates a read operation, transmitting read data during the data transfer operation;

receiving bank selection information, wherein the bank selection information identifies a bank of the plurality of banks (602, 606); and

writing the first and second data values to the memory cell array included in the bank identified by the bank selection information, wherein the first and second data values are written during the write operation."

XII. Claim 1 of auxiliary request IV differs from claim 1 of auxiliary request III in that the following text is inserted before the words "characterized by":

"wherein receiving command information further comprises receiving address information, wherein the address information corresponds to a storage location associated with the data;"

Reasons for the Decision

1. The appeal complies with the provisions referred to in Rule 101 EPC and is therefore admissible.

2. *The parent application*

2.1 The parent application is directed to a protocol for communicating data between a memory controller 601, connected to a CPU 600, and a dynamic random access memory (DRAM) 603 over a memory channel 622, as shown in Figure 6. The memory channel comprises a nine-bit data bus (BusData[8:0]), a bus control line (BusCtl) and a bus enable line (BusEnable). In addition, it includes a "clock from master" line 628 aligned with

request and write data packets transmitted by the controller, and a "clock to master" line 630 aligned with read data packets transmitted by the DRAM (see page 7, line 14, to page 8, line 6, of the description of the published parent application).

2.2 As explained on page 9, line 13, to page 10, line 28, with reference to Figure 8, the memory controller initiates a memory operation by transmitting, over the bus control and data lines, a request packet comprising control information specifying a data transfer operation (read or write) and a first memory location of the data to be transferred. The data transfer operation starts at the first location and continues at additional locations transmitted over the bus enable line. The end of the operation is signalled by a terminate indication transmitted by the controller on the bus control line.

2.3 In order to increase utilisation of the memory channel, data packets and control information are dynamically interleaved, i.e. the time period between transmission of the control information and the start of the data transfer is allowed to be flexible in order to provide time for transmitting, for example, control information for other memory operations. This is achieved by letting the transfer of data begin upon transmission of a strobe signal by the memory controller on the bus control line (see page 10, line 29, to page 11, line 3, and page 12, lines 14 to 24).

3. *Main request - Article 76(1) EPC*

3.1 According to the statement of grounds of appeal, claim 1 of the main request is based on various passages of the description of the parent application,

on Figures 6 to 9, and on Appendices A and C. In what follows, references to "the description" are to be understood as references to the description of the parent application as published.

3.2 Claim 1 is directed to a method of operating a semiconductor memory device that receives an "external clock signal". The appellant argued that the expression "external clock signal" referred to the clock signal on the "clock from master" line 628 shown in Figure 6 and discussed in the description on page 7, lines 15 to 17, and page 7, line 27, to page 8, line 6. That clock signal was an external clock signal and was received and used by DRAM 603 as disclosed on page 8, lines 22 to 30.

The Board agrees that the clock signal on the "clock from master" line is a clock signal that is external to and received by DRAM 603. The passages referred to by the appellant hence disclose a specific semiconductor memory device, namely a DRAM, that receives a specific external clock signal, namely the clock signal on "clock from master" line 628 shown in the block diagram of Figure 6.

3.3 It may be questioned whether these passages provide a basis for the more general feature "a semiconductor memory device that receives an external clock signal". This concern was raised in the communication accompanying the summons to oral proceedings, together with similar concerns in respect of other claim features which, at least *prima facie*, appear to be generalisations of features and of combinations of features disclosed in the parent application. However, the Board will not pursue those concerns further and

will instead focus on the objection raised by the Examining Division.

3.4 According to the Examining Division, the parent application did not disclose the features of claim 1 "sampling the data in response to receiving an external strobe signal, wherein first and second data values of the data are sampled, in succession, during a clock cycle of the external clock signal". In particular, there was no direct and unambiguous disclosure of a successive sampling of two data values during one clock cycle of an external clock signal.

3.5 According to the appellant, this combination of features was derivable from Appendix A.

Appendix A contains a "transaction template" showing the information that is communicated over the memory channel together with the internal DRAM core states that occur during a series of transactions. According to the first paragraph on page 35, each row of the template represents "a clock cycle or two bus samples". In addition, each row represents "4ns at 500MHz or 3.75ns at 533MHz". It follows from the discussion on page 35 that cycles 23 to 26 (see page 37) correspond to the transfer of an "octbyte" from the DRAM to the memory controller in response to a request packet specifying a "read" operation (cycle 5). Similarly, cycles 48 to 51 (see page 38) correspond to the transfer of an "octbyte" from the memory controller to a DRAM in response to a request packet specifying a "write" operation (cycle 40). The passage on page 30, lines 2 to 23, and Appendix C disclose similar information.

According to the appellant, Appendix A showed an octbyte, i.e. eight bytes, being transferred in four clock cycles over BusData[8:0] lines, even though only one byte of eight bits could be transferred over these lines at a time. This meant that one byte was sampled during each odd and each even phase of a clock cycle. In other words, two data values were sampled in succession during a clock cycle.

3.6 The appellant further referred to Figure 9, which illustrates the control information contained in a request packet. It shows six rows corresponding to "clock cycles" 0E, 0O, 1E, 1O, 2E and 2O. According to page 9, lines 20 to 22, Figure 9 corresponds to three clock cycles having even and odd phases.

3.7 In its decision, the Examining Division accepted that two bytes were sampled per row of the transaction template of Appendix A. It considered, however, that it was not directly and unambiguously derivable that one row corresponded to a clock cycle of the external clock signal.

The description on page 8, lines 22 to 26, disclosed that clock generator 618 of an I/O section of DRAM 603 used external clock signals to create clock signals for internal use by DRAM 603, and that receiver 620 and transmitter 616 of the same I/O section contained multiplexing and storage hardware to permit the internal data paths of DRAM 603 to operate "at a slower clock rate, but equivalent bandwidth, to bus lines 626".

The Examining Division further drew attention to section 1.0 of Appendix A, which mentioned that the transaction template showed "the information that is

communicated over a channel and the internal DRAM core states that occur during a series of transactions". In view of the passage on page 8, lines 22 to 26, this suggested that the sentence "Each row represents 4ns at 500MHz or (...)" meant that each row corresponded to two bus samples (of 2ns) at 500MHz and, equivalently, to one internal clock cycle of 4ns (at 250MHz).

3.8 To counter the Examining Division's reading of the parent application, the appellant submitted *inter alia* that the description on page 8, lines 22 to 26, did not disclose that data is sampled during one phase of a faster external clock and two phases of a slower internal clock to achieve equivalent bandwidth. In addition, this passage did not require the internal clock to be slower than the external clock, as it only "permit[ted] internal data paths to operate at a slower clock rate". If the "multiplexing and storage hardware" were not used, the internal and external clocks could run at the same speed.

3.9 In the Board's view the passage on page 8, lines 22 to 26, does disclose that the internal clock rate of DRAM 603 is lower than the external clock, as receiver 620 and transmitter 616 are disclosed as containing multiplexing and storage hardware and the term "permit" does not render their use optional. The Board further observes that the fifth to ninth columns of Appendix A represent internal DRAM states or activities (see page 17, section 1.5) and that these states change both at even cycles (see the sixth column of rows 10 and 18) and at odd cycles (see the sixth column of rows 35 and 45). Assuming that these cycles are external clock cycles and given that the states shown in the sixth column all last eight cycles (see page 18, section 1.7), one would expect a (longer) internal

clock cycle to correspond to a number of external clock cycles that divides 8 (i.e. either 2, 4 or 8). But one would then expect internal DRAM state changes to occur only at even cycles or only at odd cycles. In other words, the fact that the internal DRAM states shown in Appendix A change both at odd and at even rows appears to support the view that those rows correspond to internal clock cycles.

On the other hand, the parent application does not contain any other passage explicitly referring to the (lower) internal clock rate of DRAM 603 and it could be argued, for example, that the passage on page 8, lines 22 to 26, leaves open the possibility that internal DRAM states may change both at odd and at even "phases" of an internal clock cycle. In that case, if the bus is sampled at a rate of 500MHz, the external clock would run at 250MHz and the internal clock at 125MHz.

The Board hence agrees with the appellant that the passage on page 8 in itself is insufficient to conclude that the rows of the transaction template of Appendix A correspond to internal clock cycles, and not to external clock cycles.

3.10 Nevertheless, the parent application does not explicitly disclose that the rows of the transaction template correspond to clock cycles of an external clock signal, and the Examining Division's reading, which is not implausible, shows that a different reading is possible. Appendix A merely states that each row represents "a clock cycle or two bus samples" and does not explain what mechanism is behind this. The Board is aware of the "double data rate" technique used in modern memory designs that allows a computer bus to transfer data on both the rising and falling edges of

the clock signal controlling that bus, but the parent application makes no reference to this technique or an equivalent one.

3.11 It could be argued that the passage on page 9, lines 20 to 22, in combination with Figure 9, which mentions "three clock cycles, where each clock cycle has even and odd phases", is at least a step towards an explanation. However, Figure 5 is almost identical to Figure 9 and also shows six rows of clock cycles 0E, 0O, 1E, 1O, 2E and 2O. According to page 3, lines 28 to 31, Figure 5 illustrates control information according to a prior-art protocol and corresponds to six clock cycles.

Various explanations for this discrepancy are possible. For example, the prior-art protocol may transmit control information in six external clock cycles, alternately labelled "even" and "odd" in Figure 5, while the protocol disclosed in the parent application transmits essentially the same control information in two "phases" of three external clock cycles, for example using a "double data rate" technique. But the parent application never clarifies this. It can therefore also be argued that the clock cycles 0E, 0O, 1E, 1O, 2E and 2O of Figure 5 actually correspond to those of Figure 9, the only difference being that the description on page 3, lines 28 to 31, refers to (six) external clock cycles, whereas the description on page 9, lines 20 to 22, is to be understood as referring to (three) internal clock cycles. In the Board's view, this is at least a reasonable explanation that is not clearly contradicted by other passages of the parent application.

3.12 In the statement of grounds of appeal, the appellant gave further arguments why, contrary to the Examining Division's reading, the rows of the transaction template of Appendix A corresponded to clock cycles of an external clock signal and not of the DRAM's internal clock. As explained below, the Board does not find these arguments persuasive.

3.13 According to the appellant, Appendix A illustrated the transfer of data packets from the memory controller to the DRAM, which transfer was aligned with an external clock signal. This followed both from the description on page 7, line 27, to page 8, line 6, which disclosed that the (external) clock signal on the "clock from master" line 628 was aligned with request and write data packets transmitted by controller 601, and from the fact that the DRAM had no control over when data packets were sent by the memory controller, so that those packets could not be sent according to a clock cycle of the DRAM's internal clock.

The Board agrees that the transmission of request and write data packets is aligned with the external clock signal on the "clock from master" line; this is explicitly stated in the passage of the description referred to by the appellant. However, this does not mean that the rows of the transaction template necessarily correspond to clock cycles of an external clock signal. If it is the case that each row of the template corresponds to a clock cycle of the DRAM's internal clock running at half the rate of the external clock, then each row corresponds to two clock cycles of the external clock signal and no contradiction arises.

3.14 The appellant further referred to originally filed claims 5, 13, 20, 21 and 42 of the parent application,

which always refer to "clock cycle" in connection with actions of the memory controller or of the memory device or of both. According to the appellant, this implied that "clock signal" referred to an external clock signal.

However, the term "clock cycle(s)" as used in the original claims of the parent application may be understood as encompassing internal clock cycles (in particular of the DRAM), which may or may not be of the same duration as external clock cycles. The original claims are drafted at a level of abstraction at which the precise timing of signals and the relation between internal and external clock signals is not important.

3.15 The appellant submitted that "clock from master" line 628 and the plurality of lines 626 including the BusEnable line, the BusCtl line and the nine-bit data bus BusData[8:0] corresponded to the first four columns of the transaction template of Appendix A: "Clk Cyc", "BE", "BC", "BD[8:0]".

The Board notes that there is no reason why the column "Clk Cyc" should refer specifically to the "clock from master" line. While the appellant is correct in stating that request and write data packets transmitted by the memory controller to the DRAM are aligned with the clock signal on the "clock from master" line, the passage on page 7, line 27, to page 8, line 6, also discloses that read data packets transmitted by the DRAM to the memory controller are aligned with the clock signal on the "clock to master line". The Board understands that the appellant is of the view that this column in any event corresponds to external clock cycles, but this is exactly the point at issue.

3.16 The appellant argued that page 16, first paragraph, confirmed that Appendix A illustrated the timing of data transfer operations sent from "the controller to the DRAM over the BusCtl line and the nine bus data lines 'BD[8:0]'".

As explained above, the data transfer operations illustrated by Appendix A are not limited to data transfers from the controller to the DRAM. The paragraph referred to by the appellant does not state otherwise; the phrase quoted by the appellant refers only to control information being sent at clock cycles 4 through 6. Again, this paragraph does not contradict the possibility that the rows of the transaction template of Appendix A represent clock cycles of an internal clock.

3.17 The Board concludes that the arguments raised neither refute nor confirm either of the appellant's and the Examining Division's readings of Appendix A.

In this respect, the Board notes that knowing whether the rows of the transaction template correspond to clock cycles of an external clock signal or of an internal clock signal is immaterial for understanding the principles underlying the parent application and the invention as originally claimed in that application. The transaction templates in Appendices A, B and C are intended to illustrate a protocol for communicating data between a memory controller and a DRAM, and they serve that purpose independently of whether the bus is sampled twice per external clock cycle or twice per internal clock cycle. This may well be the reason why the parent application does not explain the mechanism that allows two bus samples per "clock cycle".

3.18 Article 76(1) EPC requires a direct and unambiguous disclosure in the parent application of the subject-matter of claim 1. Since in the present case the disclosure is ambiguous, the subject-matter of claim 1 extends beyond the content of the application as filed. The main request hence does not comply with Article 76(1) EPC.

4. *Auxiliary requests I, II, III and IV – Article 76(1) EPC*

Since the combination of features of claim 1 objected to in respect of the main request is also present in claim 1 of each of auxiliary requests I, II, III and IV, these requests likewise infringe Article 76(1) EPC.

5. *Conclusion*

Since none of the substantive requests on file is allowable, the appeal is to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

I. Aperribay R. Moufang

Decision electronically authenticated