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**Datasheet for the decision
of 1 October 2013**

Case Number: T 1035/11 - 3.5.05

Application Number: 02028629.0

Publication Number: 1324527

IPC: H04L1/00, H03M13/27

Language of the proceedings: EN

Title of invention:

Interleaving apparatus and method for symbol mapping in an HSDPA mobile communication system

Applicant:

Samsung Electronics Co., Ltd.

Headword:

Interleaved symbol mapping/SAMSUNG

Relevant legal provisions:

EPC Art. 56

RPBA Art. 13(1)

Keyword:

Admission of late-filed request (yes)

Inventive step - (no) - juxtaposition of obvious processes

Decisions cited:

Catchword:



Beschwerdekammern
Boards of Appeal
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Case Number: T 1035/11 - 3.5.05

D E C I S I O N
of Technical Board of Appeal 3.5.05
of 1 October 2013

Appellant: Samsung Electronics Co., Ltd.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted on 30 November 2010 refusing European patent application No. 02028629.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman: M. Höhn
Members: K. Bengi-Akyuerek
F. Blumer

Summary of Facts and Submissions

I. This appeal ("second appeal") is against the decision of the examining division ("second decision"), posted on 30 November 2010, to refuse European patent application No. 02028629.0 on the grounds that the prior art was not properly acknowledged (Rule 27(1)(b) EPC 1973), that the two-part form was not properly provided (Rule 29(1)(a)(b) EPC 1973), and that the subject-matter of the application lacked an inventive step (Article 56 EPC) with respect to a main request, a first auxiliary request, and a second auxiliary request, having regard to the disclosure of

D2: "Enhanced Symbol Mapping method for the modulation of Turbo-coded bits based on bit priority", 3GPP TSG RAN WG1/WG2 Joint Meeting on HSDPA, pp. 1-6, April 2001,

and the skilled person's common general knowledge as evidenced by

D7: "TS 25.212 V1.0.0", 3GPP TSG RAN WG1, Multiplexing and channel coding (FDD), pp. 1-38, April 1999.

A previous appeal ("first appeal") against the former decision of the examining division ("first decision"), posted on 16 February 2009, to refuse the present patent application on the grounds that the prior art was not properly acknowledged (Rule 42(1)(b) EPC), that the two-part form was not properly provided (Rule 43(1) EPC), and that the claims lacked clarity (Article 84 EPC) with respect to a sole request was settled by a decision, taken by this board in an entirely different composition ("the former board"), ordering that the

first decision be set aside, that the case be remitted to the examining division for further prosecution, and that the appeal fee be reimbursed following a substantial procedural violation committed by the examining division (cf. T 1123/09). As to the reasoning of that decision, the former board held *inter alia* that the appellant had the right to amend the description to acknowledge the respective prior-art documents following the objection raised by the examining division under Rule 27(1)(b) EPC 1973 (cf. point 3), that the formulation of the pending independent claims in the two-part form had to be postponed (cf. point 4), that the objected claims were clear (cf. point 6), and that the examining division had committed a substantial procedural violation in using new and unsupported principles with regard to the application of Rule 27(1)(b) EPC 1973 (Rule 42(1)(b) EPC) in that case (cf. point 8).

II. Notice of appeal was received on 10 February 2011. The appeal fee was paid on the same day. With the statement setting out the grounds of appeal, received on 8 April 2011, the appellant filed new claims according to a main request, a first auxiliary request, and a second auxiliary request. It requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request or any of the auxiliary requests. In addition, oral proceedings were requested as an auxiliary measure.

III. A summons to oral proceedings scheduled for 1 October 2013 was issued on 11 July 2013. In an annex to this summons, the board expressed its preliminary opinion on the appeal pursuant to Article 15(1) RPBA. In particular, objections were raised by the board

under Articles 123(2) and 56 EPC, in view of D2 and D7.

IV. With a letter of reply dated 30 August 2013, the appellant filed amended claims according to a main request and an auxiliary request. It also submitted arguments as to why D7 did not disclose the established distinguishing features and advised that a "more detailed explanation" would be provided during the oral proceedings.

V. Oral proceedings were held as scheduled on 1 October 2013, during which the former main and auxiliary requests were replaced by a new main request (claims 1 to 8) as a sole request in response to objections raised by the board under Articles 123(2) and 56 EPC. The main request was admitted into the appeal proceedings and its patentability was discussed.

The appellant's final request was that the decision under appeal be set aside and that a patent be granted on the basis of the main request as filed during the oral proceedings before the board. At the end of the oral proceedings, the board announced its decision.

VI. Claim 1 of the main request reads as follows:

"An apparatus for data transmission in a communication system, comprising:

a turbo encoder (220) for turbo coding data bits to generate systematic bits and parity bits;

a rate matcher (230) for rate matching the systematic bits and parity bits;

a first and second interleaver (250, 260) for

separately writing the rate-matched systematic bits and the rate-matched parity bits; and

a modulator (280) for alternately mapping bits collected from the first interleaver and the second interleaver onto one modulation symbol according to a modulation scheme,

characterized in that

the first interleaver is arranged for writing the rate-matched systematic bits row by row from a first row to a last row, and the second interleaver is arranged for writing the rate-matched parity bits row by row from a first row to a last row, wherein the first and second interleavers are arranged for then separately interleaving the systematic bits and the parity bits by performing inter-column permutation, respectively, according to a determined rule,

wherein the modulator is arranged for alternately collecting the permuted bits column by column in the first interleaver and the second interleaver, and

wherein in case that a number of the rate-matched systematic bits is too large for them to be written into the first interleaver, the excessive number of rate-matched systematic bits is written in the second interleaver."

The further independent claim 4 of the main request is directed to a corresponding method, while independent claims 7 and 8 are directed to a complementary apparatus and method, respectively.

Reasons for the Decision

1. Admissibility of the appeal

The appeal complies with the provisions of Articles 106 to 108 EPC (cf. point II above) and is therefore admissible.

2. MAIN REQUEST

Although this request was submitted during the oral proceedings before the board, i.e. at a relatively late stage of the procedure, the board admitted it into the appeal proceedings under Article 13(1) RPBA, since it was considered as a serious attempt to overcome the objections under Article 123(2) EPC raised in the board's communication under Article 15(1) RPBA and during the oral proceedings.

Claim 1 of this request differs from claim 1 of the main request underlying the appealed decision basically in that it further specifies that

- a) in case that a number of the rate-matched systematic bits is too large for them to be written into the first interleaver, the excessive number of rate-matched systematic bits is written in the second interleaver,

while the feature of former claim 1 specifying that

- b) "a size of the first interleaver and a size of the second interleaver are same, the first and second interleaving are performed respectively"

has been removed.

Claim 1 of this request is apparently based on the embodiment related to physically separated

interleavers, i.e. two separate interleaving buffers, according to the application as filed (cf. page 17, line 1 to page 21, line 14; Figs. 2 to 6). Feature a) is supported by the disclosure of page 18, lines 18-20 and claim 49 of the application as filed. The removal of feature b) is considered admissible since it does not represent an essential feature according to the original application (see e.g. page 17, lines 2-25).

Hence, the above amendments comply with the provision of Article 123(2) EPC.

2.1 Article 52(1) EPC: Novelty and inventive step

In the board's judgment, claim 1 does not meet the requirements of Article 52(1) and 56 EPC, for the following reasons:

2.1.1 The board concurs with the examining division in considering D2 as the closest prior art, since it is, like the present invention, related to priority-based symbol mapping of turbo coded bits in HSDPA (High Speed Downlink Packet Access) systems based on separately interleaving systematic (S) and parity (P) bits by physically separated interleavers (see D2, section 3, first paragraph in conjunction with Figs. 2 and 4).

2.1.2 Furthermore, the board agrees with the appellant that the difference between the subject-matter of claim 1 and that of D2 consists in that

- i) the first and second interleavers are arranged for writing the rate-matched systematic and parity bits row by row from a first row to a last row, respectively, and for separately interleaving the systematic and the parity bits by performing inter-column permutation, respectively, according

to a determined rule, and that the modulator is arranged for alternately collecting the permuted bits column by column in the first and second interleavers;

ii) in case that a number of the rate-matched systematic bits is too large for them to be written into the first interleaver, the excessive number of rate-matched systematic bits is written in the second interleaver.

Consequently, the subject-matter of claim 1 is found to be novel over D2 (Article 54 EPC).

2.1.3 As regards distinguishing feature i), no special technical effect or advantage which would go beyond the functioning of a well-known block interleaver, in particular as to using "inter-column permutations", can be derived from the relevant teaching of the original application with regard to physically separated interleavers (cf. page 19, line 19 to page 20, line 23). In terms of inter-column permutations, however, the appellant submitted at the oral proceedings before the board that it yielded the technical effect of "increasing the quality or grade of interleaving". Concerning distinguishing feature ii), the appellant argued at the oral proceedings that this feature allowed the buffer capacity of the first interleaver to be minimised and conceded that the underlying measure was contrary to the overall aim of fully separating the interleaving process according to the present invention, with the result that this aim was solved only in a non-ideal manner by feature ii). Nevertheless this was justified in specific situations in order to avoid data loss in case of small buffer sizes.

As to the objective problem to be solved by claim 1, the appellant referred to the application as filed, according to which the claimed subject-matter minimised hardware complexity with regard to the interleaver system in question (cf. page 19, lines 8-11).

2.1.4 The board first notes that the problem as defined by the appellant is considered to be too broad and thus cannot be accepted as a valid objective problem in this case, since there are a plethora of solutions to such a problem, all of them being equally possible to "minimise hardware complexity". Rather, according to the board, the above distinguishing features i) and ii) of claim 1 solve two different partial objective problems which are regarded as being

- I) how to implement the actual interleaving process in the first and second interleavers;
- II) how to avoid packet losses in the event that the first interleaver's capacity is exhausted.

2.1.5 Those objective problems I) and II), however, represent independent and unrelated technical problems, since problem I) relates to instructions for the interleaving process whereas problem II) relates to countermeasures in case of *structural* constraints (i.e. the first interleaver's capacity being too small) which are virtually not correlated to the actual interleaving process. In fact, the board concurs with the appellant's admission that the measure of feature ii) renders the solution according to feature i) no longer ideal, i.e. is in contradiction to the principle of fully separated interleavers for S and P bits. This is taken as an indication that there is no synergetic effect caused by distinguishing features i) and ii). Furthermore, both technical problems are problems with which the skilled person in the field of mobile

communication systems may typically have been faced at the application's priority date.

2.1.6 Confronted with problem I) and starting from D2, the skilled person would, firstly, recognise that there are no details provided in terms of the implementation of the separate interleavers in D2. In this regard, the examining division and the appellant assumed that the interleavers of D2 randomly mixed the S and P bits. The board notes, however, that random mixing of S and P bits is only related to conventional interleaving according to D2 (see page 2, first paragraph) and not to separate interleaving of S and P bits (see section 3). Thus, the skilled person would look for other documents providing useful details on viable interleaving implementations. The board therefore finds that the skilled person in the field of mobile communication systems would indeed consider the 3GPP standard document D7, which is related to turbo-coded mobile communication systems using different interleaving implementations, in order to solve objective problem I).

From document D7, the skilled person would, at first sight, understand that the turbo-coded mobile communication systems under consideration use different interleavers ("1st interleaving"; "2nd interleaving") at different system stages, i.e. some interleavers are located *before* and other interleavers are located *after* the rate matching component (see Figs. IV-1 and IV-2). However, according to the system of D2, the interleavers for downlink packet transmissions are placed after the rate matching unit (see Fig. 2). Consequently, the skilled person would take the first or second interleaver for the downlink operation of D7 (see Fig. IV-2) as a basis for implementing the

respective interleavers of D2. In this context, the board agrees with the appellant's argument submitted at the oral proceedings before the board that the internal interleaver ("mother interleaver") of the channel coding unit ("turbo coder"), also described in D7 (see page 15, line 1 to page 17, line 2 in conjunction with Fig. IV-7), cannot be taken as support for the implementation of the interleavers of D2, since it is located before the rate matching unit (see Figs. IV-1 and IV-2).

Figure IV-10 of D7 clearly illustrates in terms of the second interleaver that the incoming rate-matched bits (see "L bits" at the input side) are written row by row from a first row (row "0") to a last row (row "(N-1)M") into the corresponding interleaver matrix ("L[NxM]") of a block interleaver and that the interleaved bits are then alternately collected column by column for subsequent data modulations (see "L bits" at the output side). Furthermore, the skilled person would know from his common general knowledge that any block interleaver typically performs a kind of interleaving permutations to protect the transmitted data against burst errors, otherwise it would not qualify as an "interleaver" in the respective art. However, from the interleaving pattern exemplified for the block interleaver in D7 (see Table IV-4, sixth column), no precise and concrete type of permutations can cogently be deduced.

In this regard, the board cannot subscribe to the view of the examining division that reading the columns of the interleaving matrix from the right to the left rather than from the left to the right would already correspond to "inter-column permutation" (cf. appealed decision, page 5, last two paragraphs), since such inter-column permutations would be typically performed

during the *reading* operation, i.e. after the actual interleaving operation, rather than during the *interleaving* process. Nonetheless, in principle, there are four different variants of such permutations known to the skilled person, namely inter/intra-column or inter/intra-row permutations related to data interleaving. In this respect and contrary to the view of the appellant, the board finds that all those variants may well be considered as equally suitable alternatives, since they are substantially subject to the same processing time and complexity while providing the same effect of "increasing the quality or grade of interleaving". Moreover, the skilled person would also be aware from his common general knowledge that the underlying HSDPA referred to in D2 relies on *transport-layer* channels and that for such systems inter-column permutation is considered as a preferred choice in standard mobile communication systems (see e.g. D7, page 18, item (c), second paragraph: "The 1st interleaving is carried out on a per-transport-channel basis" in conjunction with Fig. IV-8 which shows that inter-column permutations at least for matrix columns C_1 to C_m are performed). As a consequence, the skilled person would readily apply the teaching of D7 to the system of D2 in order to implement the individual interleavers of D2, taking inter-column permutation into consideration without the need for inventive skills, and thus arrive at the solution of feature i).

2.1.7 Concerning feature ii), the skilled person would firstly recognise that, in essence, there are only two, mutually exclusive solutions in the event that a buffer happens to be too small to accommodate the respective bits, namely either accepting that the excessive bits are discarded and irreversibly lost or diverting them to another buffer, if available. Confronted with

problem II) and starting from D2, the board however considers that the skilled person would have only one solution at his disposal, i.e. to write the excessive bits into the buffer which may accommodate those bits, as required by distinguishing feature ii) - despite the fact that this solution is clearly at odds with the overall goal of separating S and P bits in the interleaving process (cf. page 5, lines 5-9 of the application as filed). Accordingly, the conclusion that only one option is suitable for solving problem II) constitutes sufficient reason why feature ii) cannot contribute to an inventive step either.

- 2.1.8 As a result, the board concludes that distinguishing features i) and ii) are associated with different technical effects and distinct partial objective problems to be solved and that their solutions constitute a mere juxtaposition of obvious processes without producing any surprising synergetic effect, since there is no combined technical effect which differs from the sum of the effects caused by the individual features solving the different partial problems I) and II). Consequently, the skilled person aiming to solve the aforementioned partial objective problems would arrive at the subject-matter of claim 1 in an obvious manner.
- 2.1.9 In view of the foregoing, the subject-matter of claim 1 does not involve an inventive step having regard to D2 combined with D7 and the skilled person's common general knowledge (Article 56 EPC).
- 2.2 In conclusion, the main request (i.e. the sole request) is not allowable under Articles 52(1) and 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:



K. Götz

M. Höhn

Decision electronically authenticated