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Datasheet for the decision of 17 September 2015

Case Number: T 0949/11 - 3.4.03

Application Number: 03090314.0

Publication Number: 1406241

IPC: G09G3/36

Language of the proceedings: EN

Title of invention:
Driving circuit and voltage generating circuit and display using the same

Applicant:
Gold Charm Limited

Headword:

Relevant legal provisions:
EPC 1973 Art. 56, 84
EPC 1973 R. 71(2)
EPC Art. 52(1), 123(2)
RPBA Art. 15(1), 15(3), 15(5), 15(6)

Keyword:
Inventive step - (no)
Amendments - added subject-matter (yes)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
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Case Number: T 0949/11 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 17 September 2015

Appellant: (Applicant)	Gold Charm Limited Offshore Chambers P.O.Box 217 Apia (WS)
Representative:	Huang, Chongguang Olswang LLP 90 High Holborn London WC1V 6XX (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 30 November 2010 refusing European patent application No. 03090314.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	S. Ward
	C. Heath

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 03 090 314 on the grounds that the subject-matter of the main request did not meet the requirements of Articles 84 and 123(2) EPC and that the subject-matter of the first auxiliary request did not meet the requirements of Article 84 EPC and did not involve an inventive step within the meaning of Article 56 EPC.

II. The appellant requested in writing that the decision under appeal be set aside, and that a patent be granted based on the main request or one of the first to fifth auxiliary requests all filed with the letter of 17 August 2015.

III. Oral proceedings before the Board were held in the absence of the appellant, the appellant having previously stated in writing that it would not attend the oral proceedings.

IV. The following documents cited by the Examining Division are referred to in this decision:

D1: US 2002/0018059 A1
D3: JP 2002 174823 A

V. Claim 1 of the main request reads as follows:

"A display unit comprising:
a substrate;
a display portion;
a gate driver circuit (3) for controlling switching of pixels of each line in the display portion (11);

a common drive circuit (4) for said display portion (11) for simultaneously driving capacitance loads in said display portion (11), wherein the common drive circuit (4) comprises:
a first voltage supply,
a second voltage supply for providing a voltage that is lower than a voltage of said first voltage supply, at least one first transistor (41) including either a drain or a source terminal connected to said first voltage supply,
at least one second transistor (42) including either a drain or a source terminal connected to said second voltage supply,
at least one signal line connected to each gate terminal of said first and second transistors (41, 42), characterized in that
said first and second transistors (41,42) are composed of thin-film transistors;
said at least one signal line conveys a common inversion signal having a high level that is substantially the same or higher than the voltage of said first voltage supply and having a low level that is substantially the same or lower than the voltage of said second voltage supply to each gate terminal of said first and second transistors (41,42);
said common drive circuit (4) further comprises a level shift (43) and a common inversion timing signal buffer (44) connected to each gate terminal of said first and second transistors (41,42);
said common inversion signal applied to each gate terminal of said first and second transistors (41,42) uses power of said gate driver circuit (3); and
respective drain and source terminals of said first and said second transistors (41,42) not connected to said first and second voltage supplies are connected to at least one capacitance load in the display portion (11),

wherein
said display portion (11), said gate driver circuit (3) and said common drive circuit (4) are mounted on the substrate (10)."

Claim 1 of the first auxiliary request is essentially the same as claim 1 of the main request except that the following feature:

"a voltage level of the gate driver circuit (3) is adapted to a voltage level of the common inversion signal;"

replaces the following feature of claim 1 of the main request:

"said common inversion signal applied to each gate terminal of said first and second transistors (41,42) uses power of said gate driver circuit (3); and".

Claim 1 of the second auxiliary request is essentially the same as claim 1 of the main request except that the following feature has been omitted:

"said common drive circuit (4) further comprises a level shift (43) and a common inversion timing signal buffer (44) connected to each gate terminal of said first and second transistors (41,42)".

The claims of the third, fourth and fifth auxiliary requests are the same as those of the main, first and second requests, respectively. These later requests differ from the first three in that figure 7 has been omitted (and the description correspondingly adapted).

VI. In a communication under Article 15(1) RPBA sent to the appellant with the summons to oral proceedings, the Board raised provisional objections under Article 123(2) and Article 84 EPC 1973, and made the following comment:

"In view of the number of objections raised above under Article 123(2) EPC and Article 84 EPC, it does not appear expedient at the present time to discuss the issues of novelty and inventive step in relation to the present requests. These matters may arise during oral proceedings."

VII. The appellant's arguments, insofar as they are relevant to the present decision, may be briefly summarised as follows:

In the light of the amendments made, all requests met the requirements of Articles 84 and 123(2) EPC.

With respect to the inventive step, the technical effect achieved by the distinguishing features was to reduce the ON resistance of the drive circuit and shorten the gate length of the transistors, enabling the circuit area to be made small.

The FETs disclosed in the closest prior art document D1 had an ON resistance small enough in order to provide the desired switching function, and thus there was no need for a further reduction of ON resistance. Document D1 actually led away from the present invention, as in Fig. 10 both FETs (FET_Y and FET_Z) were connected to the level conversion circuit (T) via respective resistors R_Y and R_Z. A further reduction of the ON resistance would remain without any effect since the resistors Ry and R_Z constituted a lower resistance bound.

The Examining Division's argument put forward in the contested decision was based on an "ex post facto" analysis. Of course, the person skilled in the art implementing the circuit of D1 directly on a panel substrate would know that thin film resistors have lower current capability than the bipolar transistors and FETs. A straightforward approach in order to compensate this lower current capability would be to provide a larger area for placing the common drive circuit.

Even though the person skilled in the art would know that an increase in gate voltage results in a reduction in channel resistance, document D1 did not give any incitation to apply this knowledge in order to reduce the ON resistance.

According to the present invention, the absolute values of the voltage level, i.e. the high and low levels of the respective signal were raised in order to drive the TFTs. Such an approach contradicted standard procedure in the art which was normally intended to reduce the applied voltage levels.

Reasons for the Decision

1. The appeal is admissible.

2. As announced in advance, the duly summoned appellant did not attend the oral proceedings. According to Rule 71(2) EPC 1973, the proceedings could however continue

without the appellant. In accordance with Article 15(3) RPBA, the board relied for its decision only on the appellant's written submissions. The board was in a position to decide at the conclusion of the oral proceedings, since the case was ready for decision (Article 15(5) and (6) RPBA), and the voluntary absence of the appellant was not a reason for delaying a decision (Article 15(3) RPBA).

3. Main Request: Articles 84 EPC 1973 and 123(2) EPC

In the light of the amendments made following the communication of the Board under Article 15(1) RPBA, the claims of the present main request are considered to meet the requirements of Article 84 EPC 1973 and Article 123(2) EPC.

4. Main Request: Inventive Step

4.1 Both the Examining Division and the appellant based their arguments in relation to inventive step on document D1, in particular on the display unit disclosed in Fig. 48 in combination with the common drive circuit disclosed in Fig. 10. The Board also considers this to be an appropriate choice of closest prior art.

4.2 It is not disputed that at least the following features of claim 1 of the main request are disclosed in document D1:

A display unit (Fig. 48) comprising a substrate (100), a display portion, a gate driver circuit (300) for controlling switching of pixels of each line in the display portion, a common drive circuit (500) for said display portion for simultaneously driving capacitance

loads in said display portion, wherein the common drive circuit comprises (see paragraph [0278] and Fig. 10):

a first voltage supply (V_Y), a second voltage supply (V_Z) for providing a voltage that is lower than a voltage of said first voltage supply (Fig. 11), at least one first transistor (FET_Y) including either a drain or a source terminal connected to said first voltage supply, at least one second transistor (FET_Z) including either a drain or a source terminal connected to said second voltage supply, wherein said common drive circuit further comprises a level shift (T) connected to each gate terminal of said first and second transistors; and wherein respective drain and source terminals of said first and said second transistors not connected to said first and second voltage supplies are connected to at least one capacitance load in the display portion.

4.3 Under point 6.1 of the contested decision, five features were identified as distinguishing claim 1 over document D1. These features (using wording closer to that of present claim 1, but retaining the numbering employed in the contested decision) are as follows:

1. the first and second transistors are composed of thin-film transistors;

2. the common inversion signal has a high level that is substantially the same or higher than the voltage of said first voltage supply;

3. the common inversion signal has a low level that is substantially the same or lower than the voltage of said second voltage supply;

4. the common inversion signal uses power of said gate driver circuit; and

5. the display portion, gate driver circuit and common drive circuit are mounted on the substrate.

The Board also considers that these features are not disclosed in the closest prior art.

4.4 Furthermore, claim 1 includes an additional distinguishing feature added in appeal:

6. the common drive circuit further comprises a common inversion timing signal buffer.

4.5 The first question which arises, therefore, is whether among these six features there is at least one which a skilled person would not consider obvious, and which, in itself, would confer an inventive character on the claimed subject-matter. If the answer to this question is negative, a further question would arise whether these features could nevertheless be considered as inventive in combination.

4.6 Document D1 discloses drive circuits (200,300,500) which are external to the display unit, as is the case in the prior art depicted in Fig. 1 of the present application. Hence, in relation to the closest prior art, the basic problem underlying the invention may be seen as reducing costs and providing high reliability. It is acknowledged in the description that a known solution is to mount at least some of the drive circuits on the LCD substrate (paragraphs [07],[10]).

Moreover, in document D3 an arrangement is disclosed in which *all* drive circuits, including the common drive

circuit 15, are mounted on the same glass substrate 11 in order to achieve *inter alia* a reduction in cost. In order to implement drive circuits on the LCD substrate, the skilled person would naturally turn to TFT technology (see e.g. document D3, paragraph [0029]). Hence, the Board considers that features 1 and 5 would be obvious to the skilled person.

4.7 Furthermore, when replacing FET_Y and FET_Z with equivalent TFT transistors, it would be obvious to the skilled person to consider additional consequential changes to adapt the circuit to TFT technology.

In general, the performance of TFTs is markedly inferior to that of conventional FETs. In particular, TFTs display a high ON resistance compared to single crystal MOSFETs. A possible approach to reducing the ON resistance of TFTs would be to increase the gate width, but this undesirably increases the circuit area, as mentioned in paragraph [11] of the description.

The problem solved by features 2 and 3 of the present invention may therefore be seen as improving the ON resistance without increasing the circuit area.

4.8 Under point 6.9 of the contested decision, the Examining Division makes the following observation:

"the low conductivity of thin-film transistors is well known. It is also well known that an increase in gate voltage results in a reduction in channel resistance. The person skilled in the art implementing the circuit of D1 directly on the panel substrate would know, therefore, how to compensate for any presumed increase in channel resistance that such an action would entail.

He would apply such compensation (by increasing gate voltage) ..."

The Board regards this as an accurate assessment, and this is also acknowledged in the statement of grounds of appeal:

"Even though the person skilled in the art would know that an increase in gate voltage results in a reduction in channel resistance ..." (page 7, paragraph 3).

A single crystal MOSFET driven to an ON state displays a correspondingly low ON channel resistance. However, an N-TFT operating at the lower end of the gate voltage range corresponding to an ON state will still display considerable ON resistance, which can be reduced by increasing the gate voltage (and vice versa for a P-TFT). Hence the skilled person would have every incentive to increase (respectively, decrease) the voltages applied to the gates of the TFTs to solve the problem of high ON resistance.

No clear explanation is given in the description why the high and low levels of the common inversion signal should be defined precisely as claimed. The Board's understanding is that the reason for providing a high level which is "the same or higher" than VCOMH, and a low level which is "the same or lower" than VCOML is simply to ensure that gate voltages are applied which are higher and lower, respectively, than the gate voltage levels which would normally be applied to FETs. As noted above, this would be an obvious measure for the skilled person to reduce the ON resistance of the TFTs, and the precise level of gate voltage would be selected according to circumstances, and without inventive activity.

4.9 The appellant argues that the claim "contradicts standard procedure" as skilled person normally attempts to reduce applied voltage levels. Although this is accurate up to a point, a more complete statement would be that the skilled person would normally try to reduce applied voltages to the most moderate levels consistent with the proper operation of the device. As noted above, it is well-known that TFTs require higher gate voltages than single crystal MOSFETs to operate optimally, and hence there is nothing which "contradicts standard procedure" in providing higher gate voltages in the present case.

For the above reasons the Board considers that features 2 and 3 would be obvious to the skilled person.

4.10 In document D1, the common inversion signal POL is derived from control circuit 600, and has a relatively small amplitude (see Figs. 11, 50A, 50B). If the FETs were replaced by TFTs, a skilled person would naturally wish to increase the amplitude of the common inversion signal to supply the appropriate high and low gate voltages referred to above.

In the opinion of the Board, an obvious possibility would be to consider deriving the power for this increased signal amplitude from existing voltage sources within the system, such as the high and low voltages of the gate driver, in order to avoid introducing additional dedicated power sources. This point was also made in the contested decision (Reasons, point 6.7) and was not challenged in the appellant's submissions. Hence, the Board considers that feature 4 would be obvious to the skilled person.

4.11 Feature 6 requires that the common drive circuit comprises a common inversion timing signal buffer. This feature is introduced in paragraph [44], but neither here nor elsewhere in the description is there any explanation of its significance or intended purpose.

Buffers in themselves are common circuit elements with well-known properties and uses, e.g. impedance matching, and a skilled person would include such an element in a design as required. In the absence of any explanation why the provision of the claimed buffer is considered to represent a non-obvious solution to a technical problem, feature 6 cannot be considered to render the claimed subject-matter inventive.

4.12 Hence, the features distinguishing claim 1 from the closest prior art cannot be seen as inventive in themselves. Furthermore, they are not seen as inventive in combination. Feature 5 sets out the fundamental idea behind the invention of mounting the drive circuits on the LCD substrate. For the reasons given above, this would be an entirely obvious measure for the skilled person, and features 1-4 merely recite equally obvious consequential adaptations to the common drive circuit. This does not represent an inventive combination of features, nor is the claimed subject-matter rendered inventive by the addition of a commonly known circuit element (feature 6), the significance of which is not explained in the application.

4.13 Concerning the arguments of the appellant in relation to the resistors R_Y and R_Z in Fig. 10 of document D1, it is noted that these resistors are provided at the gate inputs to FET_Y and FET_Z, and the appellant has not, in the opinion of the Board, fully explained why they "constitute a lower resistance bound", such that a

"further reduction of the on resistance [i.e. the drain-source resistance in the ON state] would remain without any effect".

In any event, resistors R_Y and R_Z are provided in the context of a circuit employing FET transistors. The Board is of the view that a skilled person, having decided, for the reasons set out above, to adapt the common drive circuit of Fig. 10 of document D1 to TFT technology, would be capable of making the necessary consequential changes to the circuit in the light of the known differences in characteristics and performance between the two types of transistors. In particular, the skilled circuit designer would be perfectly capable of deciding whether to retain, adapt or remove the resistors in the gate input lines following a move to a TFT-based common drive circuit. Hence, the presence of resistors R_Y and R_Z in Fig. 10 of document D1 would not represent any obstacle to the skilled person in adapting the circuit to TFT technology.

4.14 The Board therefore concludes that the subject-matter of claim 1 of the main request does not involve an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

5. First Auxiliary Request: Article 123(2) EPC

5.1 Claim 1 of the first auxiliary request includes the following feature:

- *"a voltage level of the gate driver circuit (3) is adapted to a voltage level of the common inversion signal".*

The appellant gives as basis paragraph [46] of the description which states:

"Furthermore, according to this embodiment, a common inversion signal applied to the gates of the PchTFT 41 and NchTFT 42 can use power of the gate driver circuit 3 used for the liquid crystal display. Accordingly, there is an advantage that it is no longer necessary to newly prepare a voltage level for the common drive circuit."

5.2 The claimed feature implies that, given a voltage level required for the common inversion signal, the gate driver circuit is adapted so that it outputs this required voltage. The Board can see no basis for this either in paragraph [46] or elsewhere.

What appears to be disclosed is that the common inversion signal can use the power of the gate driver, and where the voltage level of the gate driver is unsuitable, the actual voltage applied to the transistor gates can be adapted by level shift 43.

In other words, it appears that the output voltage of the level shift 43 is suitably adapted to provide the required gate voltage for the transistors. On the other hand, the voltage level of the gate driver circuit, which would appear to provide the input voltage to the level shift 43, is not disclosed in the application as filed as being in any sense "adapted".

Hence, the feature of claim 1 of the first auxiliary request that "a voltage level of the gate driver circuit is adapted ..." is not disclosed in the application as filed, and therefore the requirements of Article 123(2) EPC are not fulfilled.

6. Second Auxiliary Request

6.1 As noted above, apart from minor clarifications, claim 1 of the second auxiliary requests differs from claim 1 of the main request in that the following feature has been omitted:

6.2 "said common drive circuit (4) further comprises a level shift (43) and a common inversion timing signal buffer (44) connected to each gate terminal of said first and second transistors (41,42)".

6.3 A level shift and a buffer are no longer defined in the claim, but neither are they excluded, and so the subject-matter of claim 1 of the second auxiliary request includes the subject-matter of claim 1 of the main request, which has been found not to involve an inventive step.

6.4 The Board therefore concludes that the subject-matter of claim 1 of the second auxiliary request does not involve an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

7. Further Requests

7.1 As the claims of the third, fourth and fifth auxiliary requests are the same as those of the main, first and second requests, respectively, these requests also do not meet the requirements of the EPC, for the reasons set out above.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated