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Datasheet for the decision of 11 September 2015

Case Number: T 0332/11 - 3.4.01

Application Number: 99118897.0

Publication Number: 1006478

IPC: G06K19/07, G07F7/10, G06F12/14

Language of the proceedings: EN

Title of invention:
IC card and data updating method for IC card

Patent Proprietor:
Kabushiki Kaisha Toshiba

Opponent:
Giesecke & Devrient GmbH

Headword:

Relevant legal provisions:
EPC Art. 100(a)
RPBA Art. 13(1)

Keyword:
Inventive step - (no)
Late-filed auxiliary requests - admitted (no)

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Catchword:

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Case Number: T 0332/11 - 3.4.01

D E C I S I O N
of Technical Board of Appeal 3.4.01
of 11 September 2015

Appellant: (Patent Proprietor)	Kabushiki Kaisha Toshiba 1-1 Shibaura 1-chome, Minato-ku Tokyo 105-8001 (JP)
Representative:	Kramer Barske Schmidtchen Patentanwälte PartG mbB European Patent Attorneys Landsberger Strasse 300 80687 München (DE)
Respondent: (Opponent)	Giesecke & Devrient GmbH Prinzregentenstrasse 159 81677 München (DE)
Representative:	Bornhäuser, Frank Giesecke & Devrient GmbH Prinzregentenstraße 159 D-81677 München (DE)
Decision under appeal:	**Decision of the Opposition Division of the European Patent Office posted on 9 December 2010 revoking European patent No. 1006478 pursuant to Article 101(3)(b) EPC.**

Composition of the Board:

Chairman	G. Assi
Members:	F. Neumann
	D. Rogers

Summary of Facts and Submissions

I. The appeal lies from the decision of the opposition division revoking European patent number 1 006 478.

II. The opposition was filed against the patent in its entirety and based on the grounds of Article 100(a) EPC 1973 (lack of inventive step), Article 100(b) EPC 1973 and Article 100(c) EPC 1973.

The opponent cited *inter alia* the following documents:
D4: US-A-5 200 600; and
D5: Handbuch der Chipkarten, W. Rankl / W. Effing, 2nd Edition, 1996.

The European patent was revoked on the basis that the subject-matter of claims 1 and 9 of the main request (patent as granted) extended beyond the content of the application as filed (Article 100(c) EPC 1973) and that claims 1 and 9 of both of the auxiliary requests underlying the decision had been amended in such a way as to extend the protection they conferred (Article 123(3) EPC).

III. With the statement setting out the grounds of appeal, the appellant (proprietor) requested that the decision under appeal be set aside and the patent be maintained as granted (main request).

Alternatively, the appellant requested that the patent be maintained in amended form on the basis of one of the sets of claims making up the first and second auxiliary requests filed on 22 November 2010 during the oral proceedings before the opposition division.

Despite the fact that the contested decision dealt only with Article 100(c) EPC 1973 and Article 123(3) EPC, in the statement setting out the grounds of appeal the appellant addressed all of the issues which had been raised in the notice of opposition. Arguments were provided not only with regard to added subject matter but also with regard to sufficiency of disclosure and inventive step.

IV. In reply thereto, the respondent (opponent) requested that the appeal be dismissed.

The arguments of the respondent focused on amendments and disclosure of the invention.

In view of the fact that the contested decision did not deal with novelty and inventive step, the respondent suggested that it would be appropriate to remit the case to the opposition division for the assessment of these issues. Nevertheless, as a precaution, reference was made to the arguments presented in the notice of opposition in this respect.

V. Oral proceedings were requested by both parties.

The Board issued a summons to oral proceedings and sent a communication in preparation thereof. In this communication the Board made some preliminary observations with respect to added subject-matter. The Board also indicated its preliminary intention to limit the discussion at the oral proceedings to Article 100(c) EPC 1973 (patent as granted), Article 123(2) EPC (patent as amended) and Article 123(3) EPC and, if necessary, to remit the case to the opposition division for consideration of novelty and inventive step.

VI. In response to the Board's communication the respondent indicated that it would not attend the oral proceedings.

VII. In response to the Board's communication the appellant filed three new sets of claims forming the basis of new auxiliary requests I, II and III.

The appellant also indicated that it considered it appropriate to deal with novelty and inventive step in the current appeal proceedings.

VIII. During the oral proceedings, the appellant withdrew all three pending auxiliary requests and filed a new set of claims 1 to 12 forming the basis of a new auxiliary request I.

IX. The final requests of the parties were therefore as follows:

The appellant (proprietor) requested that the decision under appeal be set aside and that the opposition be rejected (main request) or, alternatively, that the patent be maintained as amended on the basis of claims 1 to 12 of Auxiliary Request I filed during the oral proceedings before the Board.

The respondent (opponent) requested that the appeal be dismissed.

X. Independent claim 1 of the appellant's main request reads as follows:

"*An IC card (12) including a volatile memory (22) and a nonvolatile memory (23) and having a function of*

loading an application in the nonvolatile memory (23), characterized by
setting means (21) adapted for setting a buffer region in both the volatile memory (22) and the nonvolatile memory (23); and
processing means (21) adapted for performing chain processing between request communication and response communication which use the buffer region set by the setting means,
said setting means (21) divides the buffer region in both the volatile memory (22) and the nonvolatile memory (23) into divisional areas each divisional area having a predetermined capacity, the nonvolatile memory (23) including a plurality of the divisional areas, and performs control so as to use the divisional areas in the nonvolatile memory (23) in a circulatory manner, when data are written from the divisional area of the volatile memory into the nonvolatile memory (23)."

Independent claim 1 of the appellant's auxiliary request I reads:

"*An IC card (12) including a volatile memory (22) and a nonvolatile memory (23) and having a function of loading an application in the nonvolatile memory (23), characterized by*
setting means (21) adapted for setting a buffer region in both the volatile memory (22) and the nonvolatile memory (23); and
processing means (21) adapted for performing chain processing between request communication and response communication which use the buffer region set by the setting means,
said setting means (21) divides the buffer region in both the volatile memory (22) and the nonvolatile memory (23) into divisional areas each divisional area

having a predetermined capacity and structure corresponding to that of the other divisional areas, the volatile memory (22) including one divisional area and the nonvolatile memory (23) including a plurality of divisional areas, and performs control so as to use the divisional areas in the nonvolatile memory (23) in a circulatory manner, when data are written from the divisional area of the volatile memory into the divisional areas of nonvolatile memory (23)."

Both requests contain an independent claim 9 which is directed to a data updating method for an IC card. The wording of these claims is not relevant for the present decision and so is not reproduced here.

Claims 2 to 8 and 10 to 12 in both requests are all dependent claims.

XI. The arguments of the parties, insofar as they are pertinent to the present decision, are set out below in the reasons for the decision.

Reasons for the Decision

1. The appeal is admissible.

2. Appellant's main request (patent as granted)

2.1 Article 100(c) EPC 1973

2.1.1 During the oral proceedings, the Board indicated its provisional opinion that the subject matter of the contested patent did not extend beyond the content of the application as filed. On this basis, the discussion at the oral proceedings focused on the question of

inventive step. In view of the fact that the subject-matter of independent claim 1 of both requests was found to lack an inventive step (see below), it is not necessary to address the issue of Article 100(c) EPC in the present decision.

2.2 Article 100(b) EPC 1973

2.2.1 The respondent submitted that the term "*chain processing*" used in independent claims 1 and 9 of the contested patent was not a recognised term and its meaning was not apparent from the patent specification. Despite the similarity to the term "*Blockverkettung (chaining)*" used in the text book D5, there was nothing in the contested patent which would suggest that this was in fact the intended meaning. The invention was therefore not disclosed in a manner sufficiently clear and complete for it to be carried out by a skilled person.

2.2.2 The Board disagrees.

As argued by the appellant, the Board considers that it would be clear to the skilled person in the context of claims 1 and 9 that "*chain processing*" is intended to refer to the so-called "*Blockverkettung*" in the sense explained on pages 182-183 of D5.

2.3 Article 100(a) EPC 1973 (inventive step)

2.3.1 The respondent took the view that the IC card defined in claim 1 of the contested patent as granted comprised a number of structural and functional features which were known from D5, a text book covering all aspects of smart card technology.

The Board agrees.

A basic IC card is depicted on Figure 2.5 on page 32 of D5. It comprises a volatile RAM, a non-volatile EEPROM and a CPU. Known characteristics of such a basic card are the following:

- the provision of memory partitions (page 129, "*Speicherorganisation*" and Figure 5.7 with regard to a RAM);
- the ability to perform atomic operations (page 150, "*atomare Abläufe*") ensuring that only complete data sets can be written in the EEPROM;
- the cyclic structure of the EEPROM buffer (page 151, penultimate paragraph, "zy*klisch aufgebaut*") to permit circulatory control and thus to reduce the write/erase stress for the EEPROM; and
- the block chaining functionality (page 182, "*Blockverkettung*") permitting the transfer of data blocks larger than the size of the transmitting and receiving buffers.

2.3.2 The appellant did not contest these findings and conceded that D5 disclosed all features of claim 1 (in combination) except the following:

a) the buffer region of the volatile memory (RAM) is divided into a number of divisional areas, each divisional area having a predetermined capacity;
b) the buffer region of the non-volatile memory (EEPROM) is also provided with several divisional areas, each divisional area having a predetermined capacity; and
c) the setting means is adapted to set the divisional areas in the volatile and non-volatile memories.

2.3.3 Having particular regard to feature b) above, the respondent pointed to the known drawback associated with frequent writing of data to the buffer of the EEPROM, namely the limited lifetime of the EEPROM, and indicated that D5 teaches that this drawback would be avoided by the circulatory control mentioned above (page 151, penultimate paragraph).

The appellant acknowledged this disclosure but considered that this was by no means a disclosure of multiple divisional areas of a predetermined capacity in the buffer of the EEPROM.

The Board observes that the fact that the card of D5 uses the circulatory control mentioned above is a clear indication that the buffer of the EEPROM of D5 does in fact include a number of divisional areas which are each written to in turn to alleviate the write stress of the EEPROM.

That these areas have a "*predetermined capacity*" is also clear. D5 explains that the buffer area is created so as to be large enough to accept all of the data to be written there (page 150, penultimate paragraph). The capacity of the buffer areas may therefore be considered to be "*predetermined*" in the sense of determined in advance. Whether or not the divisional areas in the EEPROM of D5 are the same size as the divisional areas of the RAM is of no significance, since this is not a limitation which is derivable from the term "*predetermined capacity*" in claim 1.

Hence, feature b) identified above is also known from D5.

2.3.4 As a result, the subject-matter of claim 1 is distinguished from the IC card known from D5 only in that the setting means is adapted to divide the buffer region of the volatile memory into a number of divisional areas, each divisional area having a predetermined capacity.

The appellant submitted that the presence of various divisional areas in the buffer region of the volatile memory would enable prioritisation of one region over another when the data is written to the non-volatile memory. The actual speed of data writing would not be increased but the management of the writing process could nevertheless be improved.

2.3.5 The Board notes that, besides the limited lifetime of the EEPROM, a further disadvantage discussed in D5 is the relatively long write and erase times of the EEPROM, as compared to a RAM (see page 130, paragraph 4). This disadvantage is particularly pertinent when using the block chaining functionality mentioned above.

When large amounts of data are to be transmitted to the card, the data to be sent is partitioned into smaller individual blocks which are sent to the card one after the other. If the card's receive buffer in the RAM is not large enough to store all of the data passed using block chaining, the data must be moved to the EEPROM. This leads to a sharp reduction in the transmission rate since the EEPROM (in contrast to the RAM) cannot be written at the full speed of the processor (page 183, lines 25-27). However, none of the passages of D5 cited by the respondent suggest a solution to this problem.

The skilled person, starting from a basic IC card as known from D5 and attempting to use block chaining, would therefore realise that the slow write time of the EEPROM leads to a bottleneck in the data flow.

2.3.6 In order to solve this problem, the skilled person would turn to D4 which recognises the problem and provides a solution thereto. In particular, D4 discloses an IC card and a method for writing information to the IC card. A problem which is discussed in D4 concerns the fact that the time required for writing data to the EEPROM is longer than the time required for writing data to the SRAM. In particular, this can prove problematic when a large amount of data has to be continuously written to the card. This problem is solved in D4 by dividing the buffer region of the SRAM into a plurality of divisional areas each having a predetermined capacity of 32 bytes (column 4, lines 59-65; column 7, lines 21-48). Whilst data is being transferred between one region of the SRAM and the EEPROM, further data blocks may be written to the other regions of the SRAM.

The skilled person would therefore realise that in order to overcome the problem of slow write times to the EEPROM, the buffer region of the volatile memory of the card should advantageously be divided into a plurality of divisional areas, each having a predetermined capacity.

2.3.7 The skilled person would therefore arrive at the subject matter of claim 1 without an inventive step.

2.3.8 The appellant understood the expression "*predetermined capacity*" as implying that the divisional areas all had the same size, this being significant for the question

of inventive step. Indeed, the fact that the data blocks were the same size made the data transfer between the volatile and non-volatile memories easier. No additional organisation was necessary because the data in the volatile memory was organised in the same manner as the data in the non-volatile memory. The management of the writing process could therefore be improved.The Board notes that it is not clearly defined in claim 1 that the divisional areas all have the same size. It is only stated that "*each divisional area*" has "*a predetermined capacity*". In the Board's view, the term "*predetermined capacity*" implies only that each divisional area has a certain capacity which is determined in advance; it does not imply that the capacity of each divisional area is necessarily the same as that of the other divisional areas.

This argument therefore does not change the above conclusion that the subject-matter of claim 1 lacks an inventive step.

2.3.9 In conclusion, the appellant's main request is not allowable.

3. Appellant's auxiliary request I (patent as amended)

3.1 Amendments

The amended claim 1 forming the basis of Auxiliary Request I was filed during the oral proceedings. The claim was essentially amended by specifying the following:

- each divisional area of the buffer region in both the volatile memory and the non-volatile memory has a predetermined capacity "*and structure*

corresponding to that of the other divisional areas";
- the volatile memory includes "*one divisional area*"; and
- data are written from the divisional area of the volatile memory into the divisional areas of the non-volatile memory.

3.2 Admissibility of the request

3.2.1 Under Article 13(1) of the Rules of Procedure of the Boards of Appeal (RPBA), it is at the Board's discretion to admit any amendment to the appellant's case after the grounds of appeal have been filed.

In accordance with established case law, one of the criteria to be considered when exercising this discretion is whether the amendments are prima facie clearly allowable. This requirement would not be fulfilled if the new claims do not overcome the objections raised against higher ranking requests (Case Law of the Boards of Appeal of the European Patent Office, 7th edition, 2013, IV.E.4.4.1-4.4.2).

3.2.2 Moreover, according to established case law, features which do not contribute to the solution of the problem set out in the description are not to be considered when assessing the inventive step of a combination of features. Only those features are to be considered which contribute causally to the solution of the problem (Case Law of the Boards of Appeal of the European Patent Office, 7th edition, 2013, I.D.9.5).

3.2.3 In the present case, the appellant has not explained how the provision of divisional areas of the same size and structure contributed to the solution of the

problem set out in paragraph [0010] of the contested patent.

The Board notes that, according to this passage, the object of the invention is to enable a reduction in the number of times data is written in a non-volatile memory and to enable general-nature atomicity management. However, the advantage associated with the identical nature of the divisional areas rather concerns the fact that the data is organised in the same manner in all of the divisional areas and could therefore be more easily transferred block-by-block from the volatile memory to the non-volatile memory. Since this amended feature does not make any contribution to solving the problem indicated in the description, this feature is not relevant for assessing the inventive step of claim 1.

3.2.4 With regard to the other two amendments made, neither of these serve to overcome the inventive step objection raised against claim 1 of the main request since both features are known from D5.

In particular, even if "*including one divisional area*" were to be interpreted as a restriction to a single divisional area, feature a) mentioned above could no longer be seen as a distinguishing feature.

Furthermore, it is clear from the chapter on atomic operations in D5 (pages 150-151) that the data is written into the divisional areas of the EEPROM. This feature is therefore also known from D5.

3.2.5 Consequently, the objection of lack of inventive step raised against claim 1 of the main request would not

overcome by claim 1 of Auxiliary Request I on a *prima facie* basis.

3.2.6 Therefore, Auxiliary Request I was not admitted into the proceedings.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

R. Schumacher G. Assi

Decision electronically authenticated