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Datasheet for the decision of 7 December 2016

Case Number: T 0315/11 - 3.4.03

Application Number: 06011118.4

Publication Number: 1863096

IPC: H01L29/06, H01L29/78, H01L29/267, H01L29/165, H01L21/04, H01L29/812, H01L29/732, H01L29/24, H01L29/20, H01L29/16

Language of the proceedings: EN

Title of invention:
Semiconductor device and method of manufacturing the same

Applicant:
Nissan Motor Company Limited

Headword:

Relevant legal provisions:
EPC Art. 52(1), 123(2)
EPC 1973 Art. 56

Keyword:
Inventive step - (yes)

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

Decisions cited:

Catchword:

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Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 0315/11 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 7 December 2016

Appellant: (Applicant)
Nissan Motor Company Limited
2 Takara-cho
Kanagawa-ku
Yokohama-shi, Kanagawa 221-0023 (JP)

Representative:
Grünecker Patent- und Rechtsanwälte
PartG mbB
Leopoldstraße 4
80802 München (DE)

Decision under appeal:
Decision of the Examining Division of the European Patent Office posted on 30 August 2010 refusing European patent application No. 06011118.4 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman G. Eliasson
Members: S. Ward
T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 06 011 118 on the grounds that the claimed subject-matter either did not involve an inventive step within the meaning of Articles 52(1) and 56 EPC (main request and first and third auxiliary requests) or was not new within the meaning of Articles 52(1), 54(1) and 54(2) EPC (second auxiliary request).

II. The Board issued a communication pursuant to Rule 100(2) EPC indicating that it was minded not to admit the main request filed with the statement of grounds of appeal into the proceedings under Article 12(4) RPBA, and that the subject-matter of the claims of the auxiliary request filed with the statement of grounds of appeal appeared to satisfy the requirements of the EPC.

III. In the letter dated 20 October 2016 the appellant withdrew the main request, and requested that the decision under appeal be set aside, and that a patent be granted based on:

- claims 1 and 2 of the auxiliary request filed with the statement of grounds of appeal;

- description: pages 3-8 as originally filed, pages 1, 1a, 2 and 10 filed with the letter of 21 June 2007, and page 9 filed with the letter of 23 April 2009;

- drawings: sheets 1/2 - 2/2 as originally filed.

IV. The following documents are referred to in this decision:

D2: HAJJIAH A T ET AL: "Novel SiC-Trench-MOSFET with Reduced Oxide Electric Field" SOLID-STATE AND INTEGRATED CIRCUITS TECHNOLOGY, 2004, PROCEEDINGS, 18 October 2004, pages 340-344, XP010805392

D6: CHEN XINGBI: "Theory of a Novel Voltage Sustaining (CB) Layer for Power devices" CHINESE JOURNAL OF ELECTRONICS, vol. 7, no. 3, July 1998, pages 211 -216, XP000900759.

V. Claim 1 reads as follows:

"A semiconductor device, comprising:
a first conductive type semiconductor base substrate constituted by an n^+ *type substrate (2) and an* n^- *type drain region (1);*
the n^- *type drain region (1) formed on a first main surface of the* n^+ *type substrate (2) and having a first main surface and a second main surface opposite to the first main surface of the* n^- *type drain region (1);*
a switching mechanism (6, 7, 10) which is formed on the first main surface of the n^- *type drain region (1) and switches ON/OFF of a current,*
wherein a plurality of columnar heterojunction-semiconductor regions (4), which are made of a semiconductor material having a different band gap from the semiconductor base substrate, are formed at spaced intervals within the n^- *type drain region (1), and the heterojunction-semiconductor regions (4) penetrate from the first main surface to the second main surface of the* n^- *type drain region (1);*
wherein the semiconductor base substrate is made of any one of silicon carbide (SiC), gallium nitride (GaN),

and diamond, and the heterojunction-semiconductor regions (4) are made of p^+ type polycrystalline silicon."

Reasons for the Decision

1. The appeal is admissible.

2. *Article 123(2) EPC*

2.1 Claims 1 and 2 of the sole request (the "Auxiliary Request" filed with the statement of grounds) correspond essentially to those of the main request as refused.

2.2 In the contested decision, these claims were found to meet the requirements of Article 123(2) EPC. In particular, claim 1 was judged to correspond to a combination of originally filed claims 1, 2 and 4, together with features taken from the description (page 4, lines 22-26; page 6, lines 11-13; page 9, lines 24-26) and from Figs. 1 and 2. The Board sees no reason to disagree with this assessment. Claim 2 essentially corresponds to claim 3 as originally filed. The requirements of Article 123(2) EPC are therefore met.

3. *Closest prior art*

3.1 In the contested decision, document D6 was selected as the closest prior art. For the reasons now given, the Board does not consider this to be an appropriate choice.

3.2 The present invention addresses the problem of achieving a low on-state resistance (see e.g. page 1, lines 11-19, and the passage bridging pages 1 and 2 of the description as originally filed). Document D6 also addresses this problem, and discusses the inherent limitations to reducing the on-state resistance in a silicon voltage sustaining layer. This is referred to as the "silicon limit" (see equations (1) and (2) and related text).

3.3 One known approach to this problem is to form the semiconductor device from wide band gap materials such as silicon carbide (SiC), so that the "silicon limit" is no longer an issue (see e.g. document D2, Abstract). This approach also forms part of the solution of the present claimed invention, in which the substrate is defined to be made of any one of silicon carbide (SiC), gallium nitride (GaN), and diamond.

3.4 Although wide band gap materials offer advantages in this respect, silicon offers the advantages of a familiar and mature technology. Hence an alternative approach is to persist with silicon, but to attempt to engineer a device which can "beat" the silicon limit. This is the challenge which is taken up in document D6 (see abstract), and solved by means of a device including a composite buffer layer formed of n-type silicon and p-type polysilicon (see page 215, "Conclusions and Discussion").

3.5 Starting from document D6, it is reasonable to suppose that the skilled person would consider making modifications which were consistent with the stated aim and purpose, for example, modifications aimed at beating the silicon limit by a wider margin.

The Board does not, however, find it realistic that the skilled person would start from document D6 and then abandon the core idea presented therein (a silicon device which can beat the silicon limit) in favour of an entirely different approach (the use of wide band gap materials), so that the main problem addressed in document D6 - i.e. beating the silicon limit - is no longer solved but merely avoided.

Document D6 is therefore not considered an appropriate choice of closest prior art for the present invention.

3.6 Since the claimed semiconductor device includes wide band gap materials (SiC, GaN or diamond), and since semiconductor devices based on wide band gap materials were well-known at the filing date of the present application, the Board considers that it would be artificial to start from a document which fails to disclose such materials. Among the available prior art disclosing semiconductor devices including wide band gap materials, document D2 appears to be the most suitable, and the Board therefore takes this document to be the closest prior art.

4. *Inventive step starting from document D2*

4.1 Document D2 discloses (e.g. Fig. 6 and the right hand image of Fig. 7) a semiconductor device, comprising:

a first conductive type semiconductor base substrate constituted by a substrate and an n type drain [drift] region;

the drain region formed on a first main surface of the substrate and having a first main surface and a second

main surface opposite to the first main surface of the drain region;

a switching mechanism which is formed [at least in part] on the first main surface of the drain region and switches ON/OFF of a current,

wherein a columnar heterojunction-semiconductor region, which is made of a semiconductor material having a different band gap from the semiconductor base substrate, is formed within the drain region, and the heterojunction-semiconductor region penetrates the drain region;

wherein the semiconductor base substrate is made of silicon carbide (SiC), and the heterojunction-semiconductor regions are made of p type polycrystalline silicon.

4.2 A first difference between the claimed invention and document D2 is that the base substrate is constituted by an n^+ type substrate and the drain region is constituted by an n^- type material, whereas in document D2, the corresponding doping levels are unspecified.

However, the choices according to claim 1 are considered to be entirely conventional, and cannot serve as the basis for the acknowledgement of an inventive step.

4.3 A second difference is that claim 1 defines a plurality of columnar heterojunction-semiconductor regions formed at spaced intervals within the n^- type drain region.

Once again, it is entirely conventional in power switching devices to arrange a plurality of individual

MOSFET cells on the same substrate. Providing a plurality of cells of the type shown in document D2 in Fig. 6 or on the right-hand side of Fig. 7 would result in columnar heterojunction-semiconductor regions at spaced intervals within the drift region.

4.4 A third difference is that, according to claim 1, the plurality of columnar heterojunction-semiconductor regions "penetrate from the first main surface to the second main surface of the n^- type drain region".

The problem is to provide both a high breakdown voltage and a low on resistance. This is achieved by the claimed feature in the manner explained, for example, in the passage from page 6, line 23 to page 7, line 3 of the description as filed.

4.5 In document D2 the "N-Drift" region corresponds to the claimed drain region. The claimed first main surface of the drain region can be seen to correspond to the interface between the drift layer and the p doped region beneath the source, and the claimed second main surface of the drain region can be seen to correspond to the interface between the "N-Drift" region and the substrate.

Thus, in contrast to present claim 1, document D2 discloses a p type "polysilicon trench" (corresponding to the claimed columnar heterojunction-semiconductor region) which extends from above the first main surface, and does not penetrate to the second main surface, but stops within the drift layer.

4.6 In document D2 the purpose of the p-type polysilicon trench is to relieve the electric field stress on the gate oxide. This is achieved by increasing the electric

field in the drift region under the p-trench (page 343, left-hand column, second paragraph), and particularly in the corner region of the polysilicon (page 342, left-hand column, first paragraph).

The skilled person would not therefore consider extending the polysilicon region in document D2 down to the substrate, as this would eliminate the region of the drift layer under the trench, the very feature which provides the required stress relief.

4.7 The Board therefore concludes that the subject-matter of claim 1 would not be obvious to a skilled person having regard to the state of the art, and hence this subject-matter is judged to involve an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   - claims 1 and 2 of the auxiliary request filed with the statement of grounds of appeal;

   - description: pages 3-8 as originally filed, pages 1, 1a, 2 and 10 filed with the letter of 21 June 2007 and page 9 filed with the letter of 23 April 2009;

   - drawings: sheets 1/2 - 2/2 as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated