Internal distribution code:

(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 23 January 2018

Case Number: T 0148/11 - 3.5.01

Application Number: 04753015.9

Publication Number: 1629389

IPC: G06F13/16

Language of the proceedings: EN

Title of invention:
MEMORY CHANNEL WITH BIT LANE FAIL-OVER

Applicant:
Intel Corporation

Headword:
Memory channel / INTEL CORPORATION

Relevant legal provisions:
EPC Art. 56
RPBA Art. 12(2), 12(4), 13(1), 13(3)

Keyword:
Inventive step - fail-over circuit for redirecting signals (no - known in the art)
Late-filed auxiliary requests - admitted (no)

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

Boards of Appeal

Chambres de recours

Boards of Appeal of the
European Patent Office
Richard-Reitzner-Allee 8
85540 Haar
GERMANY
Tel. +49 (0)89 2399-0
Fax +49 (0)89 2399-4465

Case Number: T 0148/11 - 3.5.01

D E C I S I O N
of Technical Board of Appeal 3.5.01
of 23 January 2018

Appellant: (Applicant)	Intel Corporation 2200 Mission College Boulevard Santa Clara, CA 95054 (US)
Representative:	Michael Hartig Boehmert & Boehmert Anwaltspartnerschaft mbB Pettenkoferstrasse 22 80336 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 27 September 2010 refusing European patent application No. 04753015.9 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	W. Chandler
Members:	N. Glaser
	C. Schmidt

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division, posted on 27 September 2010, refusing European patent application No. 04 753 015.9 pursuant to Article 97(2) EPC on the ground of Article 123(2) EPC.

II. The decision also referred to the document "IEEE Standards for High-Bandwidth Memory Interface Based on Scalable Coherent Interface (SCI) Signaling Technology (RamLink)", IEEE Standards, vol. IEEE, No. 1596.4, 19 March 1996, which had been mentioned in the proceedings as D1.

III. In the notice of appeal, the appellant requested reversal of the decision in its entirety. In the statement setting out the grounds of appeal, the appellant argued why refused claim 1 fulfilled the requirements of Article 123(2) EPC. He also repeated arguments given in examining proceedings why claim 1 was new and inventive over D1. Oral proceedings were requested in case substantial objections would remain.

IV. In a first communication the Board expressed its preliminary view that the main request contravened Article 123(2) EPC and was not clear (Article 84 EPC). The Board also stated that it could not see how a clarified claim could be novel or inventive over D1.

V. In a response the appellant filed a new main request and argued why claim 1 overcame the Board's objections.

VI. In an annex to the summons to oral proceedings, the Board expressed its preliminary opinion that the main

request still contravened Articles 123(2), 84, 54 and 56 EPC.

VII. The oral proceedings were held on 23 January 2018 during the course of which the appellant presented amended sets of claims according to a new main request and first and second auxiliary requests, replacing the previous requests on file. The Board admitted the new main request, but not the first and second auxiliary requests.

The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request or one of the first or second auxiliary requests, as filed during the oral proceedings.

At the end of the oral proceedings the Chairman announced the decision.

VIII. Independent claim 1 according to the main request reads as follows:

"1. A first memory buffer, comprising:

a redrive circuitry having a plurality of input/output (I/O) cells, each I/O cell providing a bit-lane for a channel between a second memory buffer and a third memory buffer that the first memory buffer is to reside between, wherein the channel comprises a uni-directional outbound path and a separate distinct uni-directional inbound path wherein the inbound path and the outbound path each comprise a plurality of bit-lanes, and wherein the redrive circuit comprises an outbound redrive circuit to receive and redrive signals on the outbound path and an inbound redrive circuit to

receive and redrive signals on the inbound path;

a memory interface; and

a fail-over circuit, the fail-over circuit capable of redirecting a signal from a first bit-lane of one of the unidirectional path to a second bit-lane of the one unidirectional path,

wherein the outbound redrive circuit is capable of having its redrive capability disabled if the first memory buffer is a last memory buffer on the outbound path, the disablement of the redrive capability further comprising: i) the outbound redrive circuit terminating the outbound path by not redriving an outbound signal received along the outbound path; ii) the inbound redrive circuit originating the inbound path by driving an inbound signal received from the memory interface on the inbound path rather than a signal received from another memory buffer."

IX. Claim 1 of the first auxiliary request adds to claim 1 of the main request at the end of the third feature *"in response to detecting that the second bit-lane failed when receiving a data pattern from another memory buffer"*, and replaces the last feature by *"wherein the first memory buffer is capable of constantly transmitting permuting idle patterns on the inbound path, if the first memory buffer is a last memory buffer on the outbound path and whenever the first memory buffer is not sending data that a host connected to the first memory buffer has requested from any memory devices attached to the memory interface."*

X. Claim 1 of the second auxiliary request deletes the feature from claim 1 of the first auxiliary request

that the fail-over circuit is capable of redirecting a signal in response to a failure of the second bit-lane, and recites instead "a *fail-over circuit capable of detecting that a bit-lane failed when receiving a data pattern from another memory buffer*."

XI. The appellant essentially argued as follows:

The invention was directed to a memory buffer which was connected to other memory buffers via uni-directional links on an inbound and outbound channel. In order to reduce energy consumption an outmost memory buffer, seen from the memory controller, was capable of disabling its outbound redrive circuit, whereas the inbound redrive circuit, originating in the outmost buffer, re-drove an inbound signal received from the memory interface on the inbound path, as shown in Figure 6 of the application.

This allowed the memory buffers to be spaced further apart and have a vertical chaining of RAM modules where memory modules could be easily added and removed. In contrast D1 did not disclose any redriving of data signals, but just a wired bus connection of modules on a ring. The the number of modules was limited in D1 because the data signal faded with increasing distance of a memory module from the memory controller.

The invention as set out in the first and second auxiliary requests was directed to a memory buffer with a fail-over circuit which had the ability to detect bit-lane failures based on received data patterns.

Reasons for the Decision

1. Introductory remarks

1.1 In the Board's view, the present invention address different problems of a memory architecture: the handling of fail-over, a hot insertion and removal of memory modules and a reduction of unnecessary power consumption or noise. The memory modules/memory buffers/memory agents of such an architecture communicate through a channel made up of unidirectional links, that is, each memory module is capable of redriving signals from link to link on an outbound path **and** from link to link on an inbound path; the links are implemented with parallel unidirectional bit lanes.

1.2 The first problem appears to be solved by a fail-over circuit which permits a memory module to redirect one or more signals to or from the plurality of bit-lanes, see page 13, lines 20ff. The second and third problems appear to be solved by enabling a memory module to selectively disable redrive features of a last or outmost memory module on the channel connecting the memory modules (see page 5, lines 7 to 17, page 7, lines 9 to 27) or of an inner memory module on said channel (page 21, line 3, to page 22, line 20, and page 22, line 27, to page 23, line 3).

2. Main request - Article 56 EPC

2.1 The Board interprets the memory buffer of claim 1 in light of Figures 5 and 6 as comprising a memory interface 66, a fail-over circuit (not shown in Figures 4 and 5), a redrive circuitry comprising an outbound redrive circuit 60 and an inbound redrive circuit 62, whereas the outbound redrive circuit terminates the

outbound path by not redriving an outbound signal received along the outbound path, and the inbound redrive circuit originating the inbound path by driving an inbound signal from the memory interface on the inbound path rather than a signal received from another memory buffer.

2.2 D1, Figure 1, illustrates a memory controller which controls a series of RAM modules organised as RamLink topology. The attachment points between these modules depend on the signaling standard, which are illustrated at page 12, Section 3.7. Figure 10 in Section 3.7.3 illustrates a series of memory slaves with an outgoing and an incoming link from the memory controller. Both links are described as uni-directional, at page 13, Section 4.1, with a signal on an outbound path and a signal on an inbound path, and correspond to the claimed feature of "a channel comprises a uni-directional outbound path and a separate distinct uni-directional inbound path". The feature that the "inbound path and the outbound path each comprise a plurality of bit-lanes" is disclosed in paragraphs 4 and 5 on page 13 of D1.

The last RAM module or the last slave terminates the outbound path by not transmitting the outbound signal. On the other hand an incoming link back to the memory controller is shown to originate in the last RAM module or slave. A "slave" is thereby to be understood as an entity with operational functionality, such as queuing or buffering data, page 22, Section 5.6, and creating signals, page 8, Section 3.2.3.

2.3 D1 does not disclose a fail-over circuit. This feature has the technical effect of maintaining the operation

of the memory buffer topology by covering a failure of bit-lanes on the inbound or outbound path.

2.4 Being confronted with the objective technical problem of coping with failures of bit-lanes of the inbound or outbound path, the person skilled in the art would turn to D3, Figure 1, column 3, line 39, to column 4, line 28, which discloses a fail-over switch. Moreover, a "fail-over switch" is a well-known concept in the field of networking to cope with communication failures.

2.5 The subject-matter of claim 1 does therefore not involve an inventive step over a combination of D1 with D3 (Article 56 EPC).

2.6 The appellant argued that D1 discloses a ring architecture whereas the invention does not. The Board however notes that the invention also discloses a ring organisation of the memory modules. Figures 3 and 6 of the application show how data propagates from the host to the outmost memory module on an outbound path and from the outmost memory module to the host on an inbound path; the outmost memory module implicitly having its outbound path/port disabled. This illustrates a ring organisation of memory modules and not a linear organisation, contrary to the appellant's argument.

2.7 Concerning the appellant's argument that the vertical chaining of RAM modules enables memory modules to be easily added and removed, the Board considers that the organisation of memory buffers in D1, Figures 14 and 15, illustrate hybrid system configurations, combining RingLink and SyncLink signal passing, as well as hierarchical topologies, as shown in Figure 12 of Section 4.2. The memory modules, called "memory

slaves", in Section 4.2 have a different functionality depending on their hierarchical position, that is, acting as slaves or controllers. The configuration of memory slaves can be dynamically reconfigured according to system needs after shutdown and error recovery.

3. Admissibility of Auxiliary Requests 1 and 2

3.1 Auxiliary requests 1 and 2 were filed during oral proceedings before the Board.

3.2 Under the provision of Article 12(2) RPBA the statement setting out the grounds of appeal shall contain a party's complete case. According to Articles 12(4) and 13(1)(3) RPBA, the Board has a discretion to disregard requests, facts and evidence filed after the statement setting out the grounds of appeal has been filed. The discretion shall be exercised in view of inter alia the complexity of the amended subject-matter, the current state of the proceedings and the need for procedural economy (Article 13(1) RPBA). As far as procedural economy is concerned, an amendment at a late stage in the proceedings is justifiable if it is an appropriate and immediate reaction to unforeseeable developments in the previous proceedings which do not lie in the responsibility of the party submitting the amendment. As far as the complexity of the new subject-matter is concerned, according to the established jurisprudence of the boards of appeal, amendments submitted at, or a few days before, oral proceedings should only be admitted if they are clearly allowable (cf. Case Law of the Boards of Appeal of the EPO, 8th edition 2016, VII.E. 16.1.1 and 16.4.1).

3.3 Claim 1 of the first auxiliary request entails considerable amendments including the deletion of

features (with respect to the main request) and the insertion of features based exclusively on the description (page 18, lines 11 to 12, and page 19, lines 7 to 11). The amendments, an intermediate generalisation, shift the invention to a memory buffer which is capable of detecting the fail-over of bit-lanes by transmitting permuting idle patterns.

3.4 As the claim recites only part of the features of the main request and is shifted to a different group of features (fail-over detection and signal redriving rather than disabling an outbound redrive circuit), the Board considers the claimed system as diverging subject-matter (claim hopping) which in general should not be admitted into second-instance proceedings, in particular at its final stage.

3.5 Furthermore, the Board considers claim 1 to represent subject-matter extending beyond the application as filed contrary to Article 123(2) EPC.

The operation of the fail-over circuit is illustrated in Figures 13 to 15 and explained on page 13, line 11, to page 15, line 10. Figures 14 and 15 illustrate that an additional bit lane, such as an error checking bit lane WD5 is used for re-routing the data of a failed bit lane. This avoids a loss of signal capacity by using an error checking line. There is no disclosure of a remapping of bit lanes without the use of an error checking lane. In absence of an explanation from the appellant how the fail-over circuit, shown in Figures 14 and 15, is linked to Figure 13 which illustrates a fail-over circuit in connection to a redrive circuit, and how it operates, the Board concludes that the fail-over circuit of claim 1 is not supported by the application as filed.

3.6 Claim 1 of the second auxiliary request deletes the signal redirection capability of the fail-over circuit and limits it to a mere detection of bit-lane failure.

3.7 There is no basis and no support for a fail-over circuit with the capability of detecting that a bit-lane has failed when receiving a data pattern from another memory.

Page 15, lines 4 to 7, discloses that an agent having the embodiment of a failover circuit may be designed to detect a failed bit lane. Page 16, lines 18 to 27 discloses that a host and the buffers on the modules observe the test pattern on each bit lane to check for proper bit lane operation. While it may be derived from both passages, cited by the appellant, that a memory buffer is capable of detecting a failed bit lane by receiving a data pattern, it may not be derived that a failover circuit is capable of detecting the failed bit lane.

3.8 Thus, the claims of auxiliary requests 1 and 2 are not clearly allowable. The Board is not in a position to come to a substantive conclusion on the request without extending the procedure by a considerable amount of time, which would be detrimental to procedural economy and legal certainty. The procedural circumstances do not justify such a conduct of the proceedings.

3.9 After having taken all these circumstances into account in exercising the discretion given to it in Articles 12(2)(4) and 13(1) RPBA, the Board does not admit the late-filed auxiliary requests 1 and 2 into the proceedings.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

T. Buschek W. Chandler

Decision electronically authenticated