Internal distribution code:
(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 19 May 2015

Case Number: T 0081/11 - 3.4.03

Application Number: 00966464.0

Publication Number: 1158581

IPC: H01L21/762

Language of the proceedings: EN

Title of invention:
METHOD FOR MANUFACTURING SOI WAFER, AND SOI WAFER

Applicant:
Shin-Etsu Handotai Co., Ltd.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56
EPC Art. 123(2)

Keyword:
Inventive step - (yes)

Decisions cited:

Catchword:

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 0081/11 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 19 May 2015

Appellant:
(Applicant)

Shin-Etsu Handotai Co., Ltd.
6-2, Ohtemachi 2-chome
Chiyoda-ku
Tokyo (JP)

Representative:

Wibbelmann, Jobst
Wuesthoff & Wuesthoff
Patentanwälte PartG mbB
Schweigerstrasse 2
81541 München (DE)

Decision under appeal:

Decision of the Examining Division of the European Patent Office posted on 26 October 2010 refusing European patent application No. 00966464.0 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman G. Eliasson
Members: S. Ward
T. Karamanli

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 00 966 464 on the ground that the claimed subject-matter did not involve an inventive step within the meaning of Article 56 EPC.

II. The appellant requested in writing that the decision under appeal be set aside, and that a patent be granted based on:

- Claim 1 as filed with the letter dated 7 September 2010;
- Description: pages 1-37 filed with the letter dated 17 March 2015; and
- Drawings: sheets 1/4 - 4/4 as originally filed.

III. The following documents are referred to in this decision:

D1: Tate N et al: Defect Reduction of Bonded SOI Wafers by Post Anneal Process in H_2 Ambient; 1998 IEEE INTERNATIONAL SOI CONFERENCE PROCEEDINGS (CAT NO.98CH36199) IEEE NEW YORK, NY, USA; October 1998, pages 141-142
D2: EP 0 926 718 A2
D6: JP 5 211128 A
D7: JP 10 242154 A
D8: JP 10 275905 A.

Documents D1 and D2 are cited in the contested decision; documents D6-D8 are cited in the description of the present application in the section entitled "Background Art". Document D8 corresponds to DE 197 53 494 A1 (which will be referred to as D8').

IV. Claim 1, being the single claim of the sole request, reads as follows:

- *"A method for producing an SOI wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating a wafer having an SOI layer at the micro bubble layer as a border, wherein, after the delamination step, the wafer having an SOI layer is subjected to a two-stage heat treatment in an atmosphere containing hydrogen or argon utilizing a rapid heating/rapid cooling apparatus and a batch processing type furnace, wherein the two-stage heat treatment is performed by subjecting the wafers to a heat treatment in the rapid heating/ rapid cooling apparatus and then a heat treatment in the batch processing type furnace."*

V. The Examining Division found essentially as follows:

The subject-matter of claim 1 differed from the state of the art known from document D1 only in that after the delamination step, the wafer having an SOI layer was subjected to a two-stage heat treatment, wherein the two-stage heat treatment was performed by subjecting the wafers to a heat treatment in a batch processing type furnace after a heat treatment in a rapid heating/rapid cooling apparatus.

The objective problem might therefore be regarded as providing an annealing process for SOI wafers made by the hydrogen ion delamination method, which resulted in improved quality of the SOI layer.

Document D2 (figure 4 and associated text) stated explicitly that batch type annealing resulted in a lower density of crystal originated particle (COP) defects below the surface compared to a rapid thermal annealing (RTA) process. At the same time, D2 disclosed that for surface defects the RTA process yielded better results (figure 3 and associated text). The skilled person would therefore combine the teaching of D2 with the disclosure of Dl, applying both an RTA and a batch furnace annealing treatment to reduce both surface and below-surface COP defects.

Furthermore, Dl disclosed that performing a batch type annealing treatment on thin SOI resulted in a large density of surface defects (so-called HF defects, revealed by etching in hydrofluoric acid), because H_2 etched the buried oxide through the defect in the SOI layer during the relatively slow heat up phase. Dl stated also that the same effect did not occur during an RTA treatment, because the heat up to the anneal temperature occurred much more quickly and surface defects were covered by surface diffusion of silicon atoms before the buried oxide could be attacked by H_2. Hence, when combining an RTA with a furnace annealing step, the skilled person would first perform the RTA step, and then the furnace annealing step.

Consequently, the person skilled in the art would arrive at a solution falling within the scope of claim 1 without using inventive skill.

VI. The appellant's arguments may be briefly summarised as follows:

The distinguishing feature between the presently-claimed method and the method as disclosed in document Dl was that the wafer having an SOI layer was subjected to the claimed two-stage heat treatment. The objective problem was to provide an SOI wafer made by the hydrogen ion delamination method with improved surface quality. In particular, the invention improved (reduced) short and long period surface roughness.

According to the present invention, the surface roughness of short periods was first improved in a heat treatment by a rapid heating/rapid cooling apparatus and then the surface roughness of long periods was improved by a heat treatment utilizing a batch processing type furnace resulting in an overall improved wafer surface quality. This solution would not be rendered obvious by a combination of documents Dl and D2.

Document Dl disclosed a method in which a post H_2 anneal was carried out by an RTA process resulting in the annihilation of HF defects on SOI layers. In addition, document Dl disclosed that the RTA process was effective to reduce "secco etch defects". Document D1 contained no teaching or suggestion to perform a second heat treatment as the first heat treatment via RTA was considered completely sufficient to reduce several defects and to therewith obtain an improved SOI wafer surface. Furthermore, document Dl described the disadvantages of heat treatments in batch processing type furnaces.

Document D2 also did not disclose a two-stage heat treatment, but taught that a heat treatment should either be carried out either in a batch processing type furnace or in a rapid heating/rapid cooling apparatus.

In fact, document D2 explicitly disclosed the high cost and the low productivity of batch wise heat treatments. Similarly, none of the other prior art documents cited during the examination proceedings disclosed a two-stage heat treatment during post anneal wafer processing.

Even if there were some teaching in document D2 which would motivate a skilled reader to carry out a two-stage heat treatment (which was not the case), there was no clear guidance in which order this should be carried out.

Document D2 disclosed reducing COPs in depths of up to about 0.5 µm from the surface of a wafer by performing a heat treatment in a rapid heating/rapid cooling apparatus, and that a heat treatment in a batch processing type furnace resulted in the surface layer of a wafer being etched to a thickness of up to about 0.5 µm.

From this disclosure the skilled reader would conclude that when a heat treatment in a batch processing type furnace was performed after a heat treatment in a RTA apparatus, the wafer surface in which the COPs had been reduced by the heat treatment in the RTA apparatus would be etched and removed by the heat treatment in the batch processing type furnace. Hence it would be unreasonable to perform a heat treatment in a batch processing type furnace after a heat treatment in an RTA apparatus.

Reasons for the Decision

1. The appeal is admissible.

2. Article 123(2) EPC

2.1 Claim 1 is a combination of claims 1 and 2 as filed. The description has been suitably adapted. The Board is therefore satisfied that the requirements of Article 123(2) EPC have been met.

3. Inventive step

3.1 The Examining Division considered the closest prior art to be document D1, which concerns defect reduction in SOI wafers. In particular, under point 3 of the section "Experimental and Results" it is disclosed that an SOI wafer may be formed by a "standard Smart Cut" method, and subjected to an H_2 anneal with RTA.

Claim 1 differs from this method in that the wafer having an SOI layer is subjected to a *two-stage* heat treatment involving a heat treatment in a rapid heating/rapid cooling apparatus (i.e. RTA) followed by a heat treatment in a batch processing type furnace.

3.2 According to the Examining Division the objective problem is "to provide an annealing process for SOI wafers made by the hydrogen ion delamination method, which results in improved quality of the SOI layer". It is clear from the contested decision that the expression "improved quality" is intended to refer to improved defect reduction.

3.3 Document D2 discloses H_2 annealing methods for reducing growth defects (COPs) in silicon wafers. According to paragraph [0065], "a batchwise apparatus or a RTA apparatus can be used depending on purpose". Although it is clear from figures 3 and 4 that batchwise furnace and RTA treatments achieve different effects, it is not always apparent from the description what, precisely, the nature of this difference is. Nevertheless, the Board accepts the plausibility of the Examining Division's interpretation that document D2 discloses that for COPs lying at the surface of the silicon, an RTA treatment is superior (figure 3), but for COPs lying below the surface up to a depth of about 0.5µm, a batchwise furnace treatment gives superior results (figure 4).

On this basis it was argued in the contested decision that "to reduce both surface and below-surface COP defects" it would be obvious for the skilled person to apply both RTA and batch furnace annealing to the SOI wafer of document D1. Furthermore, according to document D1 (see "Summary") it is "imagined that silicon covers an HF defect area with Si reflow induced by H_2 RTA so that BOX [buried oxide] layers are not attacked by H_2", and on this basis it was argued that the skilled person would apply the RTA heat treatment prior to the batch furnace annealing.

3.4 The Board is not persuaded by these arguments. Firstly, it must be noted that document D2 is not concerned with SOI technology at all. An SOI wafer is mentioned once in general terms in the description of the related art (paragraph [0009]), but the invention proposed in document D2 concerns reducing or eliminating COPs in a *silicon monocrystal wafer* derived from a silicon monocrystal ingot grown by the Czochralski method.

Nowhere in document D2 is it stated or suggested that the disclosed methods may be employed, or would be effective, as a post anneal process on a previously fabricated SOI wafer.

3.5 Secondly, there is no disclosure in document D2 of a two-stage heat treatment combining a rapid heating/rapid cooling treatment with a batchwise treatment.

What is actually disclosed in document D2 is a method in which the parameters of the Czochralski method are suitably optimized (ingot oxygen concentration of 16 ppma or less; manufactured by pulling at a growth rate of 0.6 mm/min or more), and a wafer is prepared from this ingot.

The wafer thus prepared is then subjected to an anneal heat treatment *either* at 1200°C or above for one second or more through use of a rapid heating/rapid cooling apparatus, *or* at 1200°C or above for 30 minutes or more through use of a batchwise heat treatment furnace (see abstract, claims 1,2). There is no suggestion of using both heat treatments on the same wafer.

3.6 The argument in the contested decision therefore amounts to suggesting that a skilled person seeking to improve the quality of the SOI layers of document D1 would look to document D2, a document which is not concerned with SOI technology, and would thereby arrive at a solution based on a two-stage heat treatment, a feature which is not disclosed in document D2.

In fact, the only reference in either document to subjecting an SOI wafer to conventional (batch) furnace annealing stresses the disadvantages of such a measure,

in that it does not effectively annihilate HF defects on an SOI layer, and appears to lead to etching of the BOX layer by hydrogen (D1, point 2 of "Experimental and Results" and "Summary").

3.7 The comment in document D1 (see "Summary") that it is "imagined" that silicon reflow accounts for the fact that oxide layers are not etched during RTA is merely a speculative attempt to explain an observed phemomenon. To read more than that into it, in particular that it would suggest to a skilled person the possibility of carrying out a furnace anneal after an RTA treatment which would not result in etching of the oxide layer, is simply not warranted by the text.

The Board concludes, therefore, that the method of claim 1 is not rendered obvious by the combination of documents D1 and D2.

3.8 In the section "Background Art" of the present application, the invention is presented somewhat differently (with reference to documents D6, D7 and D8) as solving the problem of reducing surface roughness of an SOI layer. According to the application, the claimed two-stage heat treatment solves this problem in that heat treatment in the rapid heating/rapid cooling apparatus improves the short period components of surface roughness, whereas heat treatment in the batch processing type furnace improves the long period components of surface roughness (page 12, second paragraph – page 13, first paragraph).

However, even if this problem were seen as being more suitable than the problem cited in the contested decision, the conclusion in relation to inventive step would be unaltered.

As solutions to the problem of surface roughness of an SOI layer document D7 suggests a furnace heat treatment, document D8/D8' suggests either a furnace heat treatment or an RTA treatment, and (if surface defects are regarded as a form of short-period surface roughness) document D1 proposes an RTA treatment and suggests that a furnace heat treatment is disadvantageous.

There is no hint in the prior art that a two-stage heat treatment as defined in present claim 1 would further reduce surface roughness, and hence the subject-matter of claim 1 could not be considered obvious on the basis of this analysis either.

3.9 The Board therefore concludes that the subject-matter of claim 1 involves an inventive step within the meaning of Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   - Claim 1 as filed with the letter dated 7 September 2010;
   - Description: pages 1-37 filed with the letter dated 17 March 2015; and
   - Drawings: sheets 1/4 - 4/4 as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated