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**Datasheet for the decision  
of 3 July 2012**

**Case Number:** T 2280/10 - 3.5.02

**Application Number:** 05753216.0

**Publication Number:** 1761997

**IPC:** H02M 3/158, H02M 1/00

**Language of the proceedings:** EN

**Title of invention:**

System and method for detecting an operational fault condition  
in a power supply

**Applicant:**

GENERAL ELECTRIC COMPANY

**Opponent:**

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**Headword:**

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**Relevant legal provisions:**

EPC Art. 56

**Relevant legal provisions (EPC 1973):**

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**Keyword:**

"Inventive step - obvious combination of known features"

**Decisions cited:**

-

**Catchword:**

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Case Number: T 2280/10 - 3.5.02

**D E C I S I O N**  
of the Technical Board of Appeal 3.5.02  
of 3 July 2012

**Appellant:**  
(Applicant)

GENERAL ELECTRIC COMPANY  
1 River Road  
Schenectady  
NY 12345 (US)

**Representative:**

Illingworth-Law, William Illingworth  
Global Patent Operation - Europe  
GE International Inc.  
15 John Adam Street  
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**Decision under appeal:**

Decision of the Examining Division of the  
European Patent Office posted 28 June 2010  
refusing European patent application  
No. 05753216.0 pursuant to Article 97(2) EPC.

**Composition of the Board:**

**Chairman:** M. Ruggiu  
**Members:** M. Léouffre  
P. Mühlens

## Summary of Facts and Submissions

- I. The applicant appealed against the decision of the examining division to refuse European patent application No. 05753216.0.
- II. On 4 May 2010 and in response to summons to attend oral proceedings in front of the examining division, the applicant filed inter alia new claims 1 and 2.
- III. With a letter dated 26 May 2010 the applicant cancelled his request for oral proceedings and requested an appealable decision according to the state of the file.
- IV. The decision of the examining division referred to the communications dated 25 June 2007 and 25 February 2010. In this last communication, the division indicated that the independent claims 1 and 6 filed with the letter of 29 October 2007 were considered as lacking an inventive step having regard to  
D1 = US 6 031 743 A; or  
D2 = US 6 473 280 B1  
in combination with common general knowledge.
- V. In a communication dated 1 February 2012 summoning the appellant to oral proceedings, the Board informed the appellant that there was no doubt about the reasons for the refusal because the wording of claims 1 and 2 filed on 04 May 2010 and of claims 1 and 2 filed on 29 October 2007 were identical.

The Board referred additionally to the following state of the art:

D3 = US 4 331 995 A

and expressed its preliminary opinion that the subject-matter of the claims 1 and 6 was obvious in view of the combination of D1 and D3.

- VI. In reply to the Board's communication, with a letter dated 8 March 2012, the appellant withdrew his request for oral proceedings and requested a decision.
- VII. With a communication posted 20 March 2012 the appellant was informed that the oral proceedings appointed for 3 July 2012 were cancelled.
- VIII. The appellant requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 and 2 filed with the letter of 4 May 2010 and claims 3 to 11 filed with the letter of 29 October 2007.
- IX. Claim 1 reads as follows:

"A method for detecting an operational fault condition in a power supply (12), the power supply having a controller (32) operably coupled to first and second switches (34, 36), the first and second switches being connected in series between a voltage source (30) and a ground node (62), wherein a first electrical node (64) is electrically coupled between the first and second switches, the first electrical node being further electrically coupled to a first end of an inductor (38), the controller configured to induce the first and second switches to apply voltage pulses to the first electrical node, the method comprising:  
monitoring a voltage at the first electrical node (64) to determine a number of voltage pulses being applied

to the first electrical node over a predetermined time interval; and

determining when a first operational fault condition has occurred when the number of voltage pulses being applied to the first electrical node over the predetermined time interval is less than or equal to a predetermined number of voltage pulses; characterized in that:

the means for monitoring a voltage comprises a resistor (84) and a capacitor (86) connected such that, when the voltage at the first electrical node has a high value, electrical current flows through the resistor to charge the capacitor; and wherein the time constant of the resistor and the capacitor is greater than one or more periods of the applied voltage pulses."

Claim 6 reads as follows:

"A system (10) for detecting an operational fault condition in a power supply (12), the power supply having a controller (32) operably coupled to first and second switches (34, 36), the first and second switches being connected in series between a voltage source (30) and a ground node (62), wherein a first electrical node (64) is electrically coupled between the first and second switches, the first electrical node being further electrically coupled to a first end of an inductor (38), the controller configured to induce the first and second switches to apply voltage pulses to the first electrical node, the method [sic] comprising: means for monitoring a voltage (46) at the first electrical node (64) to determine a number of voltage pulses being applied to the first electrical node over a predetermined time interval; and means for determining (46, 50) when a first operational

fault condition has occurred when the number of voltage pulses being applied to the first electrical node over the predetermined time interval is less than or equal to a predetermined number of voltage pulses;

characterized in that:

the means for monitoring a voltage comprises a resistor (84) and a capacitor (86) connected such that, when the voltage at the first electrical node has a high value, electrical current flows through the resistor to charge the capacitor; and wherein the time constant of the resistor and the capacitor is greater than one or more periods of the applied voltage pulses."

Claims 2 to 5, respectively claims 7 to 11, are dependent on claim 1, respectively claim 6.

X. The appellant essentially argued as follows:

Documents D1 and D2 disclosed power supply devices with fault detection circuits involving so many elements "that the fault detection circuits of D1 and D2 are themselves very likely to suffer from an operational fault condition, thus making their use for detecting a fault condition in a power supply of little use. If a fault condition is detected with the detection circuits of D1 or D2, it is likely that the fault may be in the fault detection circuits themselves rather than in the power supply that it is meant to be monitoring". The fault detection circuits were also difficult to adapt to different situations with different noise levels. The present invention required "far fewer components than the arrangements of D1 and D2, namely simply a resistor and a capacitor", and was "therefore far less likely to suffer from erroneous fault detections". The

present invention was also adaptable to different noise levels by simply replacing the resistor and capacitor.

The appellant did not comment on D3.

## **Reasons for the Decision**

1. The appeal is admissible.
2. *Novelty*

D1 discloses in figure 5 a system for detecting an operational fault condition in a power supply, the power supply having a controller (element 18) operably coupled to first and second switches S1, S2, the first and second switches being connected in series between a voltage source  $V_{in}$  and a ground node, wherein a first electrical node V(1) is electrically coupled between the first and second switches S1 and S2, the first electrical node being further electrically coupled to a first end of an inductor L1 (element 19), the controller 18 configured to induce the first and second switches to apply voltage pulses to the first electrical node (see column 1, lines 59 to 63), the system comprising a voltage pulse detection circuit (Fault Detect/Protect part of controller 18, shown on figure 3) operably coupled to the first electrical node V(1) that determines the number of voltage pulses being applied to the first electrical node over a predetermined time interval, the voltage pulse detection circuit generating a first signal (signal Fault of figure 3) indicating that a first operational fault condition has occurred when the number of voltage

pulses being applied to the first electrical node over the predetermined time interval is less than or equal to a predetermined number of pulses, i.e. one pulse in the present case (column 3, line 62 to column 4, line 20).

The subject-matter of claim 1, respectively claim 6, differs from D1 in that: "the means for monitoring a voltage comprises a resistor (84) and a capacitor (86) connected such that, when the voltage at the first electrical node has a high value, electrical current flows through the resistor to charge the capacitor; and wherein the time constant of the resistor and the capacitor is greater than one or more periods of the applied voltage pulses". The subject-matter of claim 1, respectively claim 6, is therefore considered to be new.

3. *Inventive step*

3.1 The subject-matter of claim 1, respectively claim 6, differs from D1 in that the digital circuit shown in figure 3 of D1 is replaced by an analog circuit comprising a resistor and a capacitor having a specific time constant.

The problem to be solved may be seen in providing an alternative to the digital circuit of D1 which is less sensitive to faults than the circuit of D1.

A simple analog circuit monitoring the charge of a capacitor for detecting a missing pulse is known from D3 (see figures 4 and 5A to 5K and column 3, line 57 to column 5, line 14). The capacitor 155 of D3 is charged over resistor 113 when the voltage at the output of operational amplifier 71 is positive and discharged over diode 83 when the output voltage of the



operational amplifier is low. A missing negative pulse at the output of the operational amplifier results in the capacitor voltage exceeding a reference voltage (cf. column 4, lines 35 to 37 and 51 to 62).

Therefore selecting a missing pulse detector as described in D3 to replace the digital pulse detector of the power supply circuit shown in D1 is an obvious possibility for the person skilled in the art (Article 56 EPC).

3.2 The last feature of claim 1, respectively claim 6, which defines the time constant of the resistor and the capacitor as being greater than one or more periods of the applied voltage pulses appears to rely on an arbitrary choice.

A time constant of an RC circuit is usually defined by the time for charging, respectively discharging, the capacitor to 63%, respectively 37%, of its full charge. The time constant of the RC circuit is not a condition per se to make sure that, at the end of a first pulse "the comparator maintains the fault signal (F1) at a low logic level indicating that the first fault condition has not been detected" (cf. last line of paragraph 1 of page 6 of the application). The fault detection depends solely on the comparison of the capacitor voltage with the voltage reference  $V_{ref}$  as confirmed by D3 which recites that the "time constant of resistor 113 and capacitor 115 is selected so that in the time period between pulses when capacitor 115 is being charged its voltage does not reach the reference voltage" (cf. D3, column 4, lines 42 to 47). The protection circuit could be designed and operated with a charge level determined to be larger or smaller than 63%, respectively 37%, at the end of the first or the

second pulse. The last feature of claim 1, respectively claim 6 does not therefore involve an inventive step either.

The Board considers therefore that the subject-matter of claims 1 and 6 does not involve an inventive step in the sense of Article 56 EPC having regard to document D1 taken in combination with document D3 and common general knowledge.

## **Order**

**For these reasons it is decided that:**

The appeal is dismissed.

The Registrar:

The Chairman:

U. Bultmann

M. Ruggiu