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Datasheet for the decision of 10 September 2015

Case Number: T 1942/10 - 3.4.03

Application Number: 97935790.2

Publication Number: 1014453

IPC: H01L29/868

Language of the proceedings: EN

Title of invention:
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Applicant:
MITSUBISHI DENKI KABUSHIKI KAISHA

Headword:

Relevant legal provisions:
EPC Art. 123(2)
EPC 1973 Art. 54, 56

Keyword:
Novelty - (yes)
Inventive step - (yes)

Decisions cited:

Catchword:

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Case Number: T 1942/10 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 10 September 2015

Appellant: (Applicant)	MITSUBISHI DENKI KABUSHIKI KAISHA 7-3, Marunouchi 2-chome Chiyoda-ku Tokyo 100-8310 (JP)
Representative:	Meissner, Bolte & Partner GbR Postfach 86 06 24 81633 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 28 April 2010 refusing European patent application No. 97935790.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	T. M. Häusser
	C. Heath

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division to refuse the European patent application No. 97935790 for added subject-matter, lack of clarity and lack of novelty in relation to the former main request and for lack of novelty in relation to the former auxiliary request.

II. At the oral proceedings before the board the appellant requested to set aside the decision and to grant a patent on the basis of the following documents:

- Claims 1 to 5 according to the set of claims filed during oral proceedings;
- Description pages 1-5, 8, 15-26 and 31 as originally filed before the EPO, pages 14, 27-30 as filed with letter dated 5 August 2015, and pages 6, 7, 9, 10 and 13 as filed during oral proceedings; pages 11-12 being deleted;
- Figures 1 – 23 as originally filed before the EPO.

III. Reference is made to the following documents:

D1': EP 0 709 898 A,
D2: JP 47-2730 B,
D2': DE 1 614 460 A,
D3: JP 8-46221 A.

IV. The wording of independent claim 1 is as follows (board's labelling "(a)", "(a)'" and "(b)"):

"1. A semiconductor device, comprising:
- a first semiconductor layer (1) of a first conductivity type;
- a second semiconductor layer (2) of the first conduc-

tive type comprising both a first main surface forming interface (S1) together with a main surface of the first semiconductor layer (1) and a second main surface opposed to the first main surface,
- a third semiconductor layer (3) of a second conductivity type comprising a main surface which forms a second interface (S2) together with the second main surface of the second semiconductor layer (2),

(a) wherein a second lifetime ($\tau 2$) of carriers in the second semiconductor layer (2) is smaller than a first lifetime ($\tau 1$) of carriers in the first semiconductor layer (1)

(a)' and is obtained by diffusion of a heavy metal through the semiconductor device,

wherein

(b) a resistance value in the second semiconductor layer (2) decreases monotonically from the second interface (S2) to the first interface (S1), and is obtained by ion implantation of an ion of an atom with an atomic number from 2 to 8."

V. The appellant argued essentially as follows:

a) Amendments

The amendments of 5 August 2015 in relation to present claim 1 were based on page 17, lines 1-5; page 15, lines 15-25; page 27, line 22 - page 28, line 5.

b) Sufficiency of the disclosure and support in the description

In view of the amendments of 5 August 2015, claim 1 had an appropriate scope in line with the disclosure as originally filed and related to techniques which were sufficiently disclosed in line with Article 83 EPC.

Furthermore, the description was amended to be in line with the amended claims.

c) Novelty

The structure of Figure 2 of document D1' could not be equated to feature (b) of claim 1. The variation in resistivity as implied from Figure 2, namely a variation of resistance from a medium value to a high value and back to a lowest value, did not overlap with the requirements of the claim. The claimed subject-matter was thus new over document D1'.

Reasons for the Decision

1. Amendments

Claim 1 is based on claim 1 as originally filed and on the description as originally filed (page 15, lines 15-25; page 16, lines 10-15; page 17, lines 1-5; page 27, line 22 - page 28, line 2).

Dependent claims 2-4 are based on original claims 2, 3 and 4-5, respectively. Dependent claim 5 is based on original claim 6 and on the description as originally filed (page 31, lines 21-23).

The description has been brought into conformity with the amended claims and supplemented with an indication of the relevant content of the prior art without extending beyond the content of the application as filed.

Accordingly, the board is satisfied that the amendments comply with the requirements of Article 123(2) EPC.

2. Sufficiency of the disclosure and support in the description

The objection raised by the board that the former claim 1 was worded so broadly that doubts arose whether the skilled person could put the invention into practice over the whole claimed range were overcome by the introduction of the features that the desired lifetimes are obtained by diffusion of a heavy metal (part of feature (a), i. e. feature (a)') and that the desired resistance values are obtained by implantation of ions of an atom with atomic number 2 to 8 (part of feature (b)).

Furthermore, the description has been brought in line with the amended claims.

The board is thus satisfied that the invention is disclosed in a manner sufficiently clear and complete to be performed in the whole claimed range (Article 83 EPC 1973) and that the claims are adequately supported by the description (Article 84 EPC 1973).

3. Novelty

3.1 Document D1'

3.1.1 Document D1' discloses (see column 14, line 33 - column 15, line 3; Figures 1-2) a "first embodiment" of a semiconductor diode with an N^- layer 11 of a low impurity concentration which is formed on an upper major surface of an N^+ layer 13 of a high impurity concentration. Further, a P layer 12 is formed on an

upper major surface of the N^- layer 11. The N^- layer 11 is a multilayer structure of first to third regions 11a to 11c having carrier lifetimes τ_1, τ_2 and τ_3, respectively, in the relation $\tau_2<\tau_1<\tau_3$. Due to the large lifetime τ_3 of the third region 11c, soft recovery can be implemented.

A particular method of fabricating such a diode, referred to as "fifth embodiment", is described in column 20, line 43 - column 21, line 19 with reference to Figures 11-14. In that method, the multilayer structure with the layers having different carrier lifetimes is obtained by applying a corpuscular beam of proton, helium, deuterium or the like from an upper major surface side of the P layer 12 through the P layer 12 to be stopped in the N^- layer 11. The region 11a corresponds to a passage portion of the beam and has a relatively small damage density, the second region 11b corresponds to a portion close to the stop position of the corpuscular beam and is in the vicinity of the peak position of the damage density. Finally, the region 11c is not irradiated with the corpuscular beam and has no damage. The degree of damage density influences the lifetime whereby local lifetime control is performed.

Using the wording of claim 1, document D1' discloses therefore a semiconductor device, comprising:
- a first semiconductor layer (region 11c) of a first conductivity type (N);
- a second semiconductor layer (regions 11a and 11b) of the first conductive type (N) comprising both a first main surface forming interface (interface between regions 11b and 11c) together with a main surface of the first semiconductor layer (region 11c) and a second main surface opposed to the first main surface,
- a third semiconductor layer (P layer 12) of a second

conductivity type (P) comprising a main surface which forms a second interface (interface between P layer 12 and region 11a) together with the second main surface of the second semiconductor layer (regions 11a and 11b), wherein a second lifetime (τ_1, τ_2) of carriers in the second semiconductor layer (regions 11a and 11b) is smaller than a first lifetime (τ_3) of carriers in the first semiconductor layer (region 11c) (since $\tau_2<\tau_1<\tau_3$).

3.1.2 In the appealed decision, the examining division held that the subject-matter of claim 1 of the auxiliary request pending at the time, which corresponds to present claim 1 apart from the amendments mentioned under point 2 above (heavy metal diffusion, ion implantation), was not new over document D1'. In particular, the examining division held with reference to the first embodiment diode which is fabricated using the fifth embodiment method (see points 19.4 to 19.9 of the Reasons) that a monotonically *increasing* He impurity concentration was linked to a monotonically *decreasing* resistance as could be deduced from Figure 4 of the application. As D1' showed in relation to that embodiment, a monotonically increasing He impurity concentration implicitly disclosed that the resistance value was monotonically decreasing.

3.1.3 However, Figure 4 of the application shows - apart from the spreading resistance R, which is measured experimentally - the resistivity ρ and the impurity concentration N. It is described in the description of the application that there is a "reduced value" between the resistance R and resistivity ρ or impurity concentration N and that the latter quantities can be calculated automatically once R is known (description of the application, page 19, lines 9-12). Therefore, the impurity concentration N shown in Figure 4 of the

application cannot be the Helium ion concentration since there is no simple relationship between these quantities. Rather, the impurity concentration profile N shown in Figure 4 of the present application represents the effective impurity concentration of the N-doping, which is responsible for the conduction and therefore related to the resistivity in a simple way via the electron mobility.

The examining division's interpretation of the impurity concentration N is also inconsistent with the statements in the description that the resistance is in fact increased by the He ion implantation (see page 19, line 19 - page 20, line 11; page 9, lines 20-21). Finally, it is in fact expected that the resistance *increases* with increasing He ion concentration, since the Helium ions do not contribute to the conduction as they are neither a donor nor an acceptor. Rather, the damage created by the He ion implantation creates hole and electron traps thus increasing the resistance.

Since the region 11a of the embodiment of D1' referred to above has a small damage density whereas the region 11b is in the vicinity of the peak position of the damage density and therefore has a relatively large damage density, the damage density increases and hence the resistance value *increases* from the second interface (interface between region 11a and P layer 12) to the first interface (interface between regions 11b and 11c).

Feature (b) is therefore not disclosed in document D1' in relation to the above embodiment.

Moreover, no diffusion of a heavy metal for obtaining the desired carrier lifetimes is disclosed in D1' in

relation to this embodiment. The part of feature (a) relating to the diffusion of a heavy metal, i. e. feature (a)', is therefore not disclosed in document D1' in relation to this embodiment, either.

3.1.4 The other embodiments of document D1' are not considered to be closer to the subject-matter of claim 1 than the embodiment mentioned above. In particular, in relation to the fourteenth embodiment heavy metal diffusion is mentioned merely to perform uniform lifetime control in the entire semiconductor layers but not to control the local lifetime as implied by feature (a)' (see column 26, lines 12-44).

3.1.5 In view of the above, the subject-matter of claim 1 is new over document D1'.

3.2 Document D3 / other documents

3.2.1 Document D3 discloses (see the corresponding abstract and the translation of paragraphs [0016] to [0018]) an n-type first semiconductor region 1 of low impurity concentration and an n-type second semiconductor region 2 of high impurity concentration. Furthermore, a p-type semiconductor region 3 forms a p-n junction 4 with the n-type semiconductor region 1. Platinum is diffused into the device so that the lifetime of the carriers in the n-type region in the vicinity of the p-n junction is shorter than the lifetime of the carriers deep inside the n-type region.

Using the wording of claim 1, document D3 discloses therefore a semiconductor device, comprising:
- a first semiconductor layer (region deep inside the n-type region) of a first conductivity type (n);
- a second semiconductor layer (n-type region in the

vicinity of the p-n junction 4) of the first conductive type (n) comprising both a first main surface forming interface together with a main surface of the first semiconductor layer and a second main surface opposed to the first main surface,
- a third semiconductor layer (p-type semiconductor region 3) of a second conductivity type (p) comprising a main surface which forms a second interface (p-n junction 4) together with the second main surface of the second semiconductor layer, wherein a second lifetime of carriers in the second semiconductor layer is smaller than a first lifetime of carriers in the first semiconductor layer (lifetime of the carriers in the n-type region in the vicinity of the p-n junction is shorter than the lifetime of the carriers deep inside the n-type region) and is obtained by diffusion of a heavy metal (platinum) through the semiconductor device.

However, document D3 neither mentions the resistance value of the n-type region nor ion implantation. Feature (b) is therefore not disclosed in that document.

The subject-matter of claim 1 is therefore new over document D3.

3.2.2 The remaining prior-art documents on file are not closer to the subject-matter of claim 1 than documents D1' and D3. Claims 2 to 5 are dependent on claim 1.

Accordingly, the subject-matter of claims 1 to 5 is new (Article 52(1) EPC and Article 54(1) EPC 1973).

4. Inventive step

4.1 Closest state of the art / distinguishing features

Document D3 discloses subject-matter that is conceived for the same purpose as the claimed invention and has the most relevant technical features in common with it as detailed above. Document D3 is therefore regarded as the closest state of the art.

As indicated above under point 3.2.1, the subject-matter of claim 1 differs from the semiconductor device of document D3 in comprising feature (b), i. e. a resistance value in the second semiconductor layer which decreases monotonically from the second interface to the first interface, and is obtained by ion implantation of an ion of an atom with an atomic number from 2 to 8.

4.2 Objective technical problem

The effect of feature (b) is to achieve a softer recovery characteristic, i. e. slow dissipation of the recovery current, without causing any influence on the breakdown voltage (see the description of the application, page 2, second paragraph and page 15, last paragraph). The objective technical problem is therefore to achieve this effect.

4.3 Obviousness

Document D2 had been cited in the course of the examination proceedings in relation to the assessment of inventive step. Document D2' is a family member of that document. This document is concerned with achieving fast recovery, i. e. a very quickly decaying recovery current (page 3, paragraph 2; page 5, paragraph 2; Figures 1b, 2b). One way of achieving this

object is to provide an n-type region with a doping concentration which increases exponentially with increasing distance from the p-type layer (page 6, last paragraph; Figure 4).

D2' is thus concerned with achieving the opposite effect from that of the invention. The skilled person would therefore not consider document D2' in order to solve the posed problem. Moreover, the distinguishing feature (b) is anyway not disclosed in document D2', since no ion implantation is mentioned in that document. Therefore, document D2' does not lead the skilled person to the claimed invention.

The other documents on file or the skilled person's common general knowledge do not lead the skilled person to the claimed subject-matter, either.

Therefore, the subject-matter of claim 1 involves an inventive step. Claims 2 to 5 are dependent on claim 1.

Accordingly, the subject-matter of claims 1 to 5 involves an inventive step (Article 52(1) EPC and Article 56 EPC 1973).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   - Claims 1 to 5 according to the set of claims filed during oral proceedings;
   - Description pages 1-5, 8, 15-26 and 31 as originally filed before the EPO, pages 14, 27-30 as filed with letter dated 5 August 2015, and pages 6, 7, 9, 10 and 13 as filed during oral proceedings; pages 11-12 being deleted;
   - Figures 1 – 23 as originally filed before the EPO.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated