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Datasheet for the decision of 12 March 2015

Case Number: T 1888/10 - 3.4.03

Application Number: 02290504.6

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Language of the proceedings: EN

Title of invention:
Semiconductor non volatile memory device and method of producing the same

Applicant:
Fujitsu Semiconductor Limited

Headword:

Relevant legal provisions:
EPC 1973 Art. 54(1), 56

Keyword:
Novelty - main request (no)
Inventive step - auxiliary request (yes)

Decisions cited:

Catchword:

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

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Case Number: T 1888/10 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 12 March 2015

Appellant: Fujitsu Semiconductor Limited
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted on 15 March 2010 refusing European patent application No. 02290504.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman G. Eliasson
Members: T. M. Häusser
T. Bokor

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division refusing the European patent application No. 02290504 for lack of inventive step in relation to the main request and the auxiliary request then on file.

II. At the oral proceedings before the board the appellant (applicant) submitted the following requests:

Setting aside the decision under appeal, and grant of a patent on the basis of claims 1-11 filed with the letter of 12 February 2015, titled "MAIN REQUEST",

as main request,

or alternatively on the basis of the following documents:

Description: pages 1, 14-23 as filed during the oral proceedings before the board, and pages 2-13 of the application as originally filed,
Claims: 1-10 as filed during the oral proceedings before the board, titled "first auxiliary request",
Drawings: sheets 1/35-35/35 as originally filed,

as first auxiliary request.

III. Reference is made to the following documents:

D1: US 5,841,174 A,
D3: US 6,166,953 A,
D4: JP 2001-156273 A,
D4a: US 6,368,907 B1, patent corresponding to D4.

IV. The wording of the independent claims of the main request and the first auxiliary request is as follows (board's labelling "(C)", "$(C)_a$" and the subscript in "$(d)_a$"):

Main request:

"1. A method of producing a semiconductor integrated circuit device, comprising the following steps in the following order:
(a) forming a semiconductor structure including a tunnel insulating film (12A) covering a memory cell region of a substrate (11), a first silicon film (13) covering the tunnel insulating film (12A), an insulating film (14) covering the first silicon film (13), and a gate insulating film (12C) covering a logic device region of the substrate;
(b) depositing a second silicon film (16) on the semiconductor structure formed in said step (a) so that the second silicon film (16) covers the insulating film (14) in the memory cell region and the gate insulating film (12C) in the logic device region;
(c) forming a multilayer gate electrode structure (16F) in the memory cell region by successively patterning the second silicon film (16) to serve as a control gate electrode (16A), the insulating film (14), and the first silicon film (13) in the memory cell region with the second silicon film (16) being left in the logic device region;
(d) forming a protection oxide film (18) so that the protection oxide film (18) covers the multilayer gate electrode structure (16F) in the memory cell region and the second silicon film (16) in the logic device region;
(e) forming diffusion regions (11a, 11c) in both sides of the multilayer gate electrode structure (16F) in the

memory cell region by performing ion implantation of an impurity element into the substrate (11) with the multilayer gate electrode structure (16F) and the second silicon film (16) being employed as masks;
(f) forming a gate electrode (16B, 16C) in the logic device region by patterning the second silicon film (16); and
(g) forming diffusion regions (11d, 11e, 11f, 11g) in the logic device region by performing ion implantation with the gate electrode (16B, 16C) being employed as a mask,
(h) forming a first sidewall insulating film on the protection oxide film (18) on side surfaces of the multilayer gate electrode structure (16F) and forming a second sidewall insulating film directly on side surfaces of the gate electrode (16B, 16C),
whereby a nonvolatile memory device is formed in the memory cell region and a semiconductor device is formed in the logic device region,
(C) characterized in that said step (d) forms the protection oxide film (18) by thermal oxidation."

First auxiliary request:

Claim 1 of the first auxiliary request differs from claim 1 of the main request in that features (d) and (C) are replaced by the following features $(d)_a$ and $(C)_a$, respectively:

"$(d)_a$ forming a protection oxide film (18) by thermal oxidation so that the protection oxide film (18) covers the multilayer gate electrode structure (16F) in the memory cell region and the second silicon film (16) in the logic device region;"

"$(C)_a$ wherein

- the logic device region comprises first and second device regions;
- said step (a) forms first and second gate insulating films (12B, 12C) in the first and second device regions, respectively, the second insulating film (12C) being thicker than the first insulating film (12B);
- said step (f) forms first and second gate electrodes (16B, 16C) in the first and second device regions, respectively, by patterning the second silicon film (16); and
- said step (g) forms diffusion regions (11d, 11e, 11f, 11g) in the first and second device regions by employing the first and second gate electrodes (16B, 16C) being employed as masks, respectively."

V. The appellant argued essentially as follows:

(a) Main request - novelty

In Figure 3(d) of document D4 it was illustrated that the second implant protection film 22, which corresponded to the claimed protection oxide film 18, was formed on the isolation insulating film 2, which was a silicon oxide film. This was also shown in Figure 3(c). Since it was impossible to transform the oxide in place into a silicon oxide film, the second implant protection film had to be formed by *deposition* rather than by thermal oxidation, which was indicated in the description of D4a.

Moreover, it had not been disclosed in document D4a that the multilayer gate electrode structure and the gate electrode were employed as masks when the diffusion regions were formed in the memory cell region

and in the logic device region, respectively (see features (e) and (g) of claim 1 of the main request).

The subject-matter of claim 1 of the main request was therefore new over document D4.

(b) First auxiliary request - inventive step

Document D4 had to be considered the closest state of the art. In order to allow two logic devices to operate with different voltages, the skilled person would follow the teaching of document D3. Indeed, given that document D3 provided a workable solution, the skilled person would abandon the method of document D4 and adopt that of document D3.

Reasons for the Decision

1. The appeal is admissible.

2. Invention and state of the art documents

2.1 The invention

The invention relates to methods of producing a semiconductor integrated circuit including a non-volatile semiconductor storage device known as "flash memory device". The integrated circuit also comprises transistors operating at a high voltage which are used in the peripheral circuits cooperating with the memory devices for the purpose of injecting electric charges into the storage device or extracting them from the devices. Additionally, the integrated circuit comprises

a high-speed logic circuit including transistors operating at low voltage.

In particular, the invention is concerned with avoiding a protection oxide film 18, which is used for preventing any leakage current being formed on the side-walls of the floating gate electrode of the storage device, to penetrate under the gate electrode 16B of the low-voltage operation transistor thus forming "bird's beaks" which shift the threshold characteristics from a desired value. This is achieved by the claimed process in which the protection oxide film is formed to cover the multilayer gate electrode structure of the storage device before the gate electrode is patterned in the low-voltage logic device region.

2.2 Document D1

Document D1 discloses in relation to the second embodiment of Figures 4A to 5C (see column 8, line 55 to column 10, line 11) the manufacture of a flash type memory cell and a peripheral high voltage device. The surface of a substrate 301 is thermally oxidized forming a silicon oxide film 303 (Figure 4A). Then, a phosphorus-doped polysilicon film 304 is formed followed by an ONO film 305. While the memory cell formation region MCF is covered with a resist 306, the ONO film 305, the polysilicon film 304 and the silicon oxide film 303 are removed at a peripheral device formation region PDF, which is then covered by a gate oxide film 307. Subsequently, a doped polysilicon film 308 and a WSi film 309 are deposited over the entire device and a resist 310 is patterned to cover the MCF region and to define a gate electrode in the PDF region (Figure 4C). Then, using the resist as a mask, the WSi film 309 and polysilicon film 308 are etched forming a

gate electrode G1. Then a post-oxidation film 311 is formed on the gate electrode G1 and the substrate 301 in the PDF region and on the WSi film 309 in the MCF region (Figure 5A). Using the resist 312 in the MCF region as a mask, the two-layer gate electrode G2 comprising a floating gate and a control gate is formed in the MCF region. Using the gates G1 and G2 as masks, arsenic ions are injected into the substrate to form source and drain formation regions. Subsequently, the resultant structure is oxidized in a dry atmosphere at 950 °C and a post-oxide film 313 is formed on the entire structure. At the same time, the arsenic ions are activated forming source and drain regions 314 and 315 (Figure 5C).

2.3 Document D3

Document D3 relates (column 43, line 56 to column 47, line 39; Figures 58A to 58I) to flash memory devices and discloses in particular a method of producing, on the same substrate, a memory cell transistor of the flash memory, high breakdown voltage NMOS and PMOS used for writing and erasing of the flash memory, and logic system NMOS and PMOS forming part of a peripheral logic circuit. A first insulating film 6 of the high breakdown voltage NMOS and PMOS and a tunnel insulating film 7 of the flash memory are formed by thermal oxidation and wet etching to have a thickness of 20 to 40 nm and 8 to 12 nm, respectively. Subsequently, a first conductive layer 8 is deposited which will serve as a floating gate electrode of the flash memory and is patterned to serve as gate electrodes of the high breakdown voltage NMOS and PMOS (Figure 58D). An inter-layer insulating film 9 is formed to be situated between the floating gate electrode and a control gate electrode of the flash memory (Figure 58E). Then,

second gate insulating films 10 are formed having a thickness of 10 to 20 nm and serving as gate insulating films of the logic system NMOS and PMOS. Subsequently, a second conductive layer 11 is formed which will serve as a control gate electrode of the flash memory and gate electrodes of the logic system NMOS and PMOS. The control gate electrode 11, inter-layer insulating film 9 and floating gate electrode 8 of the flash memory are formed through dry etching using a mask. Then an insulating film 12 is formed over the entire surface. Source and drain of the flash memory are formed by implanting N-type regions 13 and P-type layers 14 using the control gate 11 as a mask (Figure 58F). Gate electrodes of the logic system NMOS and PMOS are formed through dry etching and N-type regions 16 are formed by using a mask such as photoresist, and P-type semiconductor regions 17 are formed using ion implantation (Figure 58G). Finally, after a silicon oxide film is formed over the entire surface through a CVD process, side walls 18 are formed on the gate electrodes through dry etching (Figure 58H).

2.4 Document D4

2.4.1 Document D4 discloses (see column 9, lines 6 - column 10, line 34 in the parallel patent D4a) a method of fabricating a semiconductor device containing a non-volatile memory device and a logic device, in particular CMOS transistors. First, an N-type well 5 is formed in the P-channel transistor formation region of the logic region Rlogc, and a P-type well 7 is formed in the entire memory region Rmemo and the N-channel transistor formation region of the logic region Rlogc (Figures 1(b) and 1(c)). Subsequently, a silicon oxide gate insulating film 8 is formed in the memory region Rmemo and a first polysilicon film 9 including phos-

phorus is formed by CVD, which will become a floating gate electrode of the non-volatile memory device. An ON film 10a (laminated film including an oxide film and a nitride film), which is to be formed into an inter-electrode insulating film, is deposited on the polysilicon film 9 (Figure 2(a)). Then a silicon oxide gate insulating film 14 is formed by thermal oxidation in the logic region Rlogc. At this point, the surface of the ON film 10a is also oxidized so as to be formed into an ONO film 10. Thereafter, a second polysilicon film 15 including phosphorus is formed by CVD which is to be formed into a control gate electrode of the non-volatile memory device and gate electrodes of the logic devices (Figure 3(b)). Then, the second polysilicon film 15, the ONO film 10 and the first polysilicon film 9 in the memory region Rmemo are patterned by dry etching using a "stacked gate formation mask" 16 covering the entire logic region Rlogc and a gate formation region in the memory region Rmemo, thereby forming a stacked gate of the non-volatile memory device including a control gate electrode 17, an inter-electrode insulating film 18 and a floating gate electrode 19 (Figure 3(c)).

2.4.2 The following step is described as follows (column 10, lines 35-49 in D4a):

"In this embodiment, in the procedure shown in FIG. 3(d), after removing the stacked gate formation mask 16, a gate electrode of the logic device is not formed but with allowing the second polysilicon film 15 to remain in the logic region Rlogc, the surfaces of the silicon films (including monosilicon and polysilicon films) exposed on the silicon substrate are oxidized by thermal oxidation, thereby forming a second implant protection film 22 of a silicon oxide film on the

silicon substrate in the memory region Rmemo, the stacked gate of the nonvolatile memory device and the second polysilicon film 15 remaining in the logic region Rlogc. The second implant protection film 22 is to be used as a protection film in ion implantation for forming a source/drain diffusion layer of the nonvolatile memory device."

2.4.3 It is further described (see D4a, column 10, line 50 - column 11, line 67) that a source/drain diffusion layer 24 of the non-volatile memory device is formed by using a source/drain formation mask 23 covering the entire logic region Rlogc (Figure 4(a)). Next, the second implant protection film 22 formed on the second polysilicon film 15 is removed by anisotropic etching. Part of this film remains as sidewalls on the side faces of the stacked gate of the non-volatile memory device (Figure 4(b)). Then, the second polysilicon film 15 in the logic region Rlogc is patterned by dry etching (Figure 4(c)) and an LDD diffusion layer 26, 28 is formed in the logic region Rlogc (Figures 4(d) and 5(a)). Next, a TEOS film deposited by CVD is formed by anisotropic dry etching into sidewall spacers 29 on the side faces of the stacked gate of the non-volatile memory device and the gate electrode 21 of the logic device (Figure 5(b)). Finally, ions are implanted thereby forming a source/drain diffusion layer 31, 33 of the logic devices (Figures 5(c) and 5(d)).

3. Main request - novelty over document D4

3.1 It is not contested by the appellant that document D4 discloses, using the wording of claim 1 of the main request, a method of producing a semiconductor integrated circuit device, comprising the following steps in the following order:

(a) forming a semiconductor structure including a tunnel insulating film (gate insulating film 8) covering a memory cell region (memory region Rmemo) of a substrate (N-type well 5 and P-type well 7), a first silicon film (first polysilicon film 9) covering the tunnel insulating film (gate insulating film 8), an insulating film (ONO film 10) covering the first silicon film (first polysilicon film 9), and a gate insulating film (silicon oxide gate insulating film 14) covering a logic device region (logic region Rlogc) of the substrate (N-type well 5 and P-type well 7);
(b) depositing a second silicon film (second polysilicon film 15) on the semiconductor structure formed in said step (a) so that the second silicon film (second polysilicon film 15) covers the insulating film (ONO film 10) in the memory cell region (memory region Rmemo) and the gate insulating film (silicon oxide gate insulating film 14) in the logic device region (logic region Rlogc);
(c) forming a multilayer gate electrode structure in the memory cell region (memory region Rmemo) by successively patterning the second silicon film (second polysilicon film 15) to serve as a control gate electrode (control gate electrode 17), the insulating film (ONO film 10), and the first silicon film (first polysilicon film 9) in the memory cell region (memory region Rmemo) with the second silicon film (second polysilicon film 15) being left in the logic device region (logic region Rlogc),
(d) forming a protection oxide film (second implant protection film 22) so that the protection oxide film (second implant protection film 22) covers the multilayer gate electrode structure in the memory cell region (memory region Rmemo) and the second silicon film (second polysilicon film 15) in the logic device region (logic region Rlogc);

(e)' forming diffusion regions (source/drain diffusion layer 24) in both sides of the multilayer gate electrode structure in the memory cell region (memory region Rmemo) by performing ion implantation of an impurity element into the substrate (P-type well 7) with the second silicon film (second polysilicon film 15) being employed as a mask (feature (e)' being part of claimed feature (e));
(f) forming a gate electrode (gate electrodes 21) in the logic device region (logic region Rlogc) by patterning the second silicon film (second polysilicon film 15), and
(g)' forming diffusion regions (LDD diffusion layers 26, 28) in the logic device region (logic region Rlogc) by performing ion implantation (feature (g)' being part of claimed feature (g)),
(h) forming a first sidewall insulating film (sidewall spacer 29) on the protection oxide film (second implant protection film 22) on side surfaces of the multilayer gate electrode structure and forming a second sidewall insulating film (sidewall spacers 29) directly on side surfaces of the gate electrode (gate electrodes 21), whereby a non-volatile memory device is formed in the memory cell region (memory region Rmemo) and a semiconductor device (CMOS transistors) is formed in the logic device region (logic region Rlogc).

3.2 In the method of document D4, the second implant protection film 22 is etched between steps (e) and (f) so that part of it remains on the side faces of the multilayer stacked gate structure (see D4a, Fig. 4(b) and column 10, line 61 - column 11, line 7). However, such an etching step is not excluded by the claimed production method, especially as subsequent to the production step (d) of the claimed protection oxide film, reference is only made to that film in feature

(h) where it is claimed that the sidewall insulating film is formed on the protection oxide film "on the side surfaces of the multilayer gate electrode structure". Furthermore, the purpose of the protection oxide film is to prevent leakage currents to be formed on the side-walls of the floating gate electrode pattern (see the description of the application, page 8, line 31 - page 9, line 10). Such leakage prevention is achieved also by the second implant protection film 22 of document D4 even after etching, since - as pointed out above - part of the film remains on the side faces of the multilayer stacked gate structure (see D4a, column 12, line 54 - column 13, line 5).

3.3 The appellant argued that document D4a - and consequently document D4 - did not disclose that the multilayer gate electrode structure and the gate electrode were employed as masks when the diffusion regions were formed in the memory cell region and in the logic device region, respectively.

However, it is evident from Figure 4(d) of document D4 and the corresponding part of the description (see column 10, lines 50 to 60 in document D4a) that the ion implantation results in source and drain regions 24 which are separated by the region of the P-type well 7 beneath the multilayer structure comprising the control gate electrode 17, the inter-electrode insulating film 18 and the floating gate electrode 19. The multilayer structure acts therefore as a mask during the ion implantation ensuring that the multilayer structure slightly overlaps the edges of the source and drain regions 24 and thus proper functioning of the non-volatile memory device is also ensured. Similarly, it is evident from Figures 4(d) and 5(a) of document D4 and the corresponding part of the description (see

column 11, lines 16 to 42 in document D4a) that the gate electrodes 21 act as masks during the ion implantation forming the source and drain regions 26 and 28. In fact, this manner of producing the source and drain regions of a MOSFET is very well-known and common practice in semiconductor manufacturing resulting in a so-called "self-aligned gate".

The parts of features (e) and (g) of claim 1 of the main request relating to the multilayer gate electrode structure and the gate electrode, respectively, being employed as masks are therefore also disclosed in document D4.

3.4 The appellant further argued that it was not disclosed in document D4 that the protection oxide film was formed by thermal oxidation.

3.4.1 It is however explicitly mentioned in document D4 (see point 2.4.2 above) that the second implant protection film 22, which corresponds to the claimed protection oxide film, is formed by thermal oxidation. Indeed, this is a standard technique in semiconductor manufacturing to produce thin layers of oxide, usually silicon dioxide, on the surface of a wafer. In the process described in document D4 thermal oxidation is furthermore not only described to be used to produce the second implant protection film 22, but also the gate insulating films 8 and 14 (see document D4a, column 9, lines 37 to 41 and column 10, lines 11 to 13). The board has therefore no doubt that the passage cited above under point 2.4.2 provides an accurate account of the manner in which the second implant protection film 22 is formed.

3.4.2 The appellant argued that it was illustrated in Figure 3(d) of document D4 that the second implant protection film 22 was formed on the isolation insulating film 2, which was a silicon oxide film. Since it was impossible to transform the oxide in place into a silicon oxide film, the second implant protection film had to be formed by *deposition* rather than by thermal oxidation.

However, the fact that the second implant protection film 22 is formed on the isolation insulating film 2 is not considered to be incompatible with its formation by thermal oxidation. Rather, the insulating film 2 being a silicon oxide film (see D4a, column 9, lines 6 to 12), as a result of the thermal oxidation used for forming the second implant protection film 22, the thickness of the isolation insulating film 2 increases due to the diffusion of oxygen through the silicon oxide film. Such an increase of the thickness of an oxide film upon thermal oxidation is described in the application of the invention in relation to the growth of the thermal oxide film 12C (see the description of the application, Figure 1F and page 3, last paragraph to page 4, first paragraph).

While it is true that the second implant protection film 22 and the isolation insulating film 2 are shown as distinct layers in Figures 3(d) and 4(a) of document D4, the board considers that factors like the fabrication of these films in separate process steps or the subsequent partial removal of the second implant protection film 22 (see D4a, Figure 4(b) and column 10, line 61 to column 11, line 7) may well have induced the draughtsman to represent them in this manner.

3.4.3 Feature (C) of claim 1 of the main request relating to

the protection oxide film being formed by thermal oxidation is therefore also disclosed in document D4.

3.5 Consequently, the subject-matter of claim 1 of the main request is not new in view of document D4 (Article 52(1) EPC and 54(1) EPC 1973).

4. First auxiliary request

4.1 Amendments

Claim 1 of the first auxiliary request is based on claims 16, 17 and 25 as originally filed and on the description and drawings as originally filed (page 22, lines 14-18; Figure 9G).

Dependent claims 2 to 10 of the first auxiliary request are based on original claims 18 to 24, 26 and 27, respectively. The description has been brought into conformity with the amended claims and supplemented with an indication of the relevant content of the state of the art without extending beyond the content of the application as filed.

Accordingly, the board is satisfied that the amendments comply with the requirements of Article 123(2) EPC.

4.2 Novelty

4.2.1 Document D4

In addition to the features of claim 1 of the main request referred to above under point 3, document D4 also discloses that

- the logic device region comprises first and second device regions (left and right regions of Rlogc, separated by the isolation insulating film 2);
- said step (a) forms first and second gate insulating films (silicon oxide gate insulating film 14) in the first and second device regions, respectively,
- said step (f) forms first and second gate electrodes (gate electrodes 21) in the first and second device regions, respectively, by patterning the second silicon film (second polysilicon film 15) (see D4, Figure 4(c)); and
- said step (g) forms diffusion regions (LDD diffusion layers 26, 28) in the first and second device regions by employing the first and second gate electrodes (gate electrodes 21) being employed as masks, respectively (see D4, Figures 4(d) and 5(a)).

Document D4 does not disclose that the second insulating film in the second device region is thicker than the first insulating film in the first device region (part of feature $(C)_a$).

The subject-matter of claim 1 of the first auxiliary request is therefore new over document D4.

4.2.2 Document D3

Document D3 discloses first and second gate insulating films (gate insulating films 10 and 6) in first and second device regions (regions of the logic NMOS/PMOS and the high breakdown voltage NMOS/PMOS, respectively), the second insulating film being thicker than the first insulating film (the insulating films 6 and 10 having thicknesses of 10-20 nm and 20-40 nm, respectively). However, only one of the corresponding gates

(namely gate electrode 11 of the logic NMOS/PMOS) is formed by patterning the second silicon film (second conductive layer 11), whereas the other corresponding gate (gate electrode 8 of the high breakdown NMOS/PMOS) is formed by patterning the first silicon film (first conductive layer 8). The part of feature $(C)_a$ of claim 1 of the first auxiliary request relating to step (f) forming first and second gate electrodes by patterning the second silicon film is therefore not disclosed in document D3.

Furthermore, the insulating film 12, which corresponds to the claimed protection oxide film, is deposited using a CVD process (D3, column 46, lines 4-7), rather than by the claimed thermal oxidation. The part of feature $(d)_a$ of claim 1 of the first auxiliary request relating to thermal oxidation is therefore not disclosed in document D3.

Finally, document D3 discloses a sidewall insulating film (side walls 18). However, they are depicted as being formed directly on the side surface of the multilayer gate electrode structure (control gate electrode 11, inter-layer insulating film 9 and floating gate electrode 8 of the flash memory) (Figure 58H). Document D3 is silent as to whether the insulating film 12, previously covering the multilayer gate, has been removed or not. The part of feature (h) of claim 1 of the first auxiliary request relating to the sidewall insulating film being formed on the protection oxide film on side surfaces of the multilayer gate electrode structure is therefore also not unambiguously disclosed in document D3.

The subject-matter of claim 1 of the first auxiliary request is therefore new over document D3.

4.2.3 Document D1

Contrary to the assessment in the decision under appeal (see point 9 of the Grounds) the board holds that document D1 merely discloses in relation to the second embodiment of Figures 4A to 5C, using the wording of claim 1 of the first auxiliary request, a method of producing a semiconductor integrated circuit device, comprising the following steps in the following order:
(a) forming a semiconductor structure including a tunnel insulating film (silicon oxide film 303) covering a memory cell region (memory cell formation region MCF) of a substrate (301), a first silicon film (polysilicon film 304) covering the tunnel insulating film (silicon oxide film 303), an insulating film (ONO film 305) covering the first silicon film (polysilicon film 304), and a gate insulating film (gate oxide film 307) covering a logic device region (peripheral device formation region PDF) of the substrate (301);
(b) depositing a second silicon film (polysilicon film 308 and WSi film 309) on the semiconductor structure formed in said step (a) so that the second silicon film (polysilicon film 308 and WSi film 309) covers the insulating film (ONO film 305) in the memory cell region (memory cell formation region MCF) and the gate insulating film (gate oxide film 307) in the logic device region (peripheral device formation region PDF);
(c) forming a multilayer gate electrode structure (two-layer gate electrode G2) in the memory cell region (memory cell formation region MCF) by successively patterning the second silicon film (polysilicon film 308 and WSi film 309) to serve as a control gate electrode (D1, column 9, lines 36-41), the insulating film (ONO film 305), and the first silicon film (poly-silicon film 304) in the memory cell region (memory

cell formation region MCF),
(d) forming a protection oxide film (post-oxide film 313) by thermal oxidation (in a dry atmosphere at 950 °C) so that the protection oxide film (post-oxide film 313) covers the multilayer gate electrode structure (two-layer gate electrode G2) in the memory cell region (memory cell formation region MCF);
(e) forming diffusion regions (diffusion layers 314) in both sides of the multilayer gate electrode structure (two-layer gate electrode G2) in the memory cell region (memory cell formation region MCF) by performing ion implantation of an impurity element into the substrate (301) with the multilayer gate electrode structure being employed as mask;
whereby a non-volatile memory device is formed in the memory cell region and
a semiconductor device is formed in the logic device region (column 8, lines 55-61).

However, the following steps are not considered to be disclosed in document D1 in the claimed order:

(c)' step (c) being performed with the second silicon film being left in the logic device region. Rather, in the method of D1 the gate electrode G1, which had been formed beforehand by etching the films 308 and 309, is being left in the logic device region (see column 9, lines 22-26; Figure 5A);
(d)' forming the protection film so that it covers the second silicon film in the logic device region. Rather, in the method of D1 the post-oxide film 313 covers the gate electrode G1, i.e. the patterned second silicon film (see Figure 5A);
(e)' the step (e) being performed with the second silicon film being employed as masks. Rather, the gate electrode had been formed beforehand as indicated

above;
(f) forming a gate electrode in the logic device region by patterning the second silicon film. Rather, as indicated above, the gate electrode G1 had been formed in a previous step,
(g) forming diffusion regions in the logic device region by performing ion implantation with the gate electrode being employed as a mask. Rather, the diffusion region 315 of the logic device had been generated simultaneously with the diffusion region 314 of the memory device,
(h) forming a first sidewall insulating film on the protection oxide film on side surfaces of the multilayer gate electrode structure and forming a second sidewall insulating film directly on side surfaces of the gate electrode.

Furthermore, there is no disclosure in document D1 of first and second device regions with first and second gate insulating films, respectively, the second insulating film being thicker than the first insulating film. Feature $(C)_a$ of claim 1 of the first auxiliary request is therefore not disclosed in document D1, either.

The first embodiment described in document D1 with reference to Figures 1A to 2B is even more remote in relation to the claimed subject-matter than the second embodiment referred to above.

The subject-matter of claim 1 of the first auxiliary request is therefore new over document D1.

4.2.4 Conclusion in relation to novelty

The remaining state of the art documents on file are not closer to the subject-matter of claim 1 of the first auxiliary request than documents D1, D3 and D4.

Claims 2 to 10 of the first auxiliary request are dependent on claim 1 of the first auxiliary request.

Accordingly, the subject-matter of claims 1 to 10 of the first auxiliary request is new (Article 52(1) EPC and Article 54(1) EPC 1973).

4.3 Inventive step

4.3.1 Closest state of the art

The appellant starts from document D4 as the closest state of the art. Indeed, document D4 discloses subject-matter that is conceived for the same purpose as the claimed invention, namely for providing a method of producing a semiconductor integrated circuit device, and has the most relevant technical features in common with it, as detailed under point 4.2 above. Document D4 is therefore regarded as the closest state of the art.

4.3.2 Distinguishing features, objective technical problem

It has been established above that the subject-matter of claim 1 of the first auxiliary request differs from the method of document D4 in that the second insulating film in the second device region is thicker than the first insulating film in the first device region (part of feature $(C)_a$).

The effect of this feature is to allow the semiconductor integrated circuit device to use a plurality of supply voltages (see the description of the

application, page 2, lines 1 to 3; cf. also page 8, lines 23 to 30). The objective technical problem is therefore how to achieve this effect.

4.3.3 Obviousness

Since the two transistors in the logic region Rlogc of document D4 are a pair of complementary MOSFETs, i. e. CMOS transistors (see D4a, column 1, lines 5-13 and column 8, line 32 - column 9, line 5), the skilled person would not modify only one of these MOSFETs in order to solve the posed problem. Rather, he might consider adding a further type of high-voltage MOSFETs in addition to the existing low-voltage CMOS transistors.

However, thermal oxidation of silicon is performed at high temperature, usually between 800 and 1200 °C, and the manufacture of silicon oxide films of different thicknesses using thermal oxidation is not straight-forward. Although document D3 teaches a solution to this problem, in view of the complicated sequence of manufacturing steps in both documents D3 and D4, the skilled person would be discouraged from incorporating some of the steps of document D3 into the method according to D4 as this would require modifying the other steps. However, even if the skilled person were to contemplate such a combination of the teachings of these documents, he would merely consider incorporating the manufacture of the high breakdown NMOS/PMOS in the method of document D4 in order to solve the posed problem. This would entail forming the gate insulating film of the high breakdown voltage NMOS/PMOS at the same time as the gate insulating film 8 of the memory device Rmemo of document D4 and forming the gate electrode of the high breakdown voltage NMOS/PMOS by

patterning the first polysilicon film 9 of D4. Such considerations would therefore not lead the skilled person to forming the gate electrode of the high breakdown NMOS/PMOS by patterning the second silicon film and would therefore not lead to the claimed subject-matter (see feature $(C)_a$ of claim 1 of the first auxiliary request).

The other state of the art documents on file do not contain any teaching which would lead the skilled person in an obvious manner to the claimed subject-matter, either.

Therefore, the subject-matter of claim 1 of the first auxiliary request involves an inventive step. Claims 2 to 10 of the first auxiliary request are dependent on claim 1 of the first auxiliary request.

Accordingly, the subject-matter of claims 1 to 10 involves an inventive step (Article 52(1) EPC and Article 56 EPC 1973).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent with the following documents:

   Description:
   pages 1, 14-23 as filed during the oral proceedings before the board,
   pages 2-13 of the application as originally filed,

   Claims:
   1-10 as filed during the oral proceedings before the board, titled "first auxiliary request",

   Drawings: sheets 1/35-35/35 as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated