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Datasheet for the decision of 21 August 2013

Case Number: T 1541/10 - 3.5.06

Application Number: 06076804.1

Publication Number: 1734440

IPC: G06F 9/38

Language of the proceedings: EN

Title of invention:
Processor for executing highly efficient VLIW instructions

Applicant:
Panasonic Corporation

Headword:
Processor for executing VLIW instructions/PANASONIC

Relevant legal provisions:
EPC Art. 123(2)

Relevant legal provisions (EPC 1973):
EPC Art. 56, 84, 111(1)

Keyword:
"Request for accelerated processing of appeal (allowed)"
"Added subject-matter (no)"
"Clarity (yes)"
"Support in the description (yes)"
"Inventive step (yes)"
"Remittal to the department of first instance (yes)"

Decisions cited:
-

Catchword:

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 1541/10 - 3.5.06

D E C I S I O N
of the Technical Board of Appeal 3.5.06
of 21 August 2013

Appellant: (Applicant)
Panasonic Corporation
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Jennings, Michael John
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 23 December 2009 refusing European patent application No. 06076804.1 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: D. H. Rees
Members: A. Teale
W. Sekretaruk

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division, dispatched on 23 December 2009, to refuse European patent application No. 06 076 804.1 on the basis that claim 1 of the then main and first to fourth auxiliary requests lacked essential features and was not supported by the description, Article 84 EPC 1973. The subject-matter of claim 1 of the then fifth auxiliary request was found to lack inventive step, Article 56 EPC 1973, in view of the combination of the following documents:

D1: EP 0 426 393 A2
D3: EP 0 479 390 A2.

The decision also referred to document
D2: EP 0 689 129 A1.

II. A notice of appeal was received on 23 February 2010. The appeal fee was paid on the same date.

III. A statement of grounds of appeal was received on 27 April 2010, together with amended claims according to new main and auxiliary requests and amended description pages. The appellant requested that the decision be set aside and that the application be allowed to proceed to grant on the basis of the new main and auxiliary requests. The appellant also made an auxiliary request for oral proceedings if the board considered the grounds of appeal to be insufficient, without further discussion, to set aside the decision and allow the application to proceed to grant on the basis of the main request.

IV. With a letter received on 30 April 2013 the appellant filed an amended set of claims and requested accelerated processing of this case before the boards of appeal because the appellant had "identified use of the invention by another company and the Applicant needs to protect its rights before the application/patent expires in 2018". The appellant requested that the amended set of claims replace those on file and that the board confirm that the application should now proceed to grant. The appellant also stated that it would ask for accelerated handling by the examining division if the case were remitted.

V. The application documents on file are as follows:

Description:
Pages 1, 2, 4 to 7 and 9 to 44, as received on 29 September 2006.
Page 2a, received on 25 September 2008.
Pages 3 and 8, received with the statement of grounds of appeal.

The then applicant further requested in the letter received on 25 September 2008 *inter alia* that all references in the description to "n operation fields" be amended to "m operation fields".

Claims:
1 to 11, received on 30 April 2013.

Drawings:
Sheets 1 to 16, received on 29 September 2006.

VI. The statement of claims comprises an independent claim 1 and dependant claims 2 to 11, claim 1 reading as follows:

VII. "A VLIW processor, comprising: fetch means (39) for fetching an instruction that includes a plurality of operation fields (52, 59); and a decoder unit (20) for decoding the plurality of operation fields (52, 59) in the fetched instruction in parallel with each other; the VLIW processor being characterised in that: the plurality of operation fields include a first type of operation field (52) and a second type of operation field (59 or 60), the first type of operation field (52) is located at a first predetermined position in the instruction and is composed of a control code with no operand thereof, the second type of operation field (59 or 60) is located at a second predetermined position in the instruction and is composed of an operation code and one or more operands, and the decoder unit (20) includes: a first decoder (23) for decoding the control code in the first type of operation field (52) and for controlling a control flow of a program, and a second decoder (24 or 25) for decoding the operation code in the second type of operation field (59 or 60)."

Reasons for the Decision

1. *The admissibility of the appeal*

In view of the facts set out at points I to III above, the appeal meets the admissibility criteria under the EPC and is therefore admissible.

2. *The request for accelerated processing*

2.1 In the letter received on 30 April 2013 the appellant requested accelerated processing of the present case before the boards of appeal because it had "identified use of the invention by another company and the Applicant needs to protect its rights before the application/patent expires in 2018".

2.2 According to the Notice from the Vice-President Directorate-General 3 dated 17 March 2008 concerning accelerated processing before the boards of appeal (OJ EPO 2008, 220), parties with a legitimate interest may ask the boards of appeal to deal with their appeals rapidly. Requests for accelerated processing should contain reasons for the urgency together with relevant documents, no particular form being required. According to the notice, it could be justified to allow such acceleration if infringement proceedings have been brought or are envisaged.

2.3 The circumstances described by the appellant are very similar to the example given in the notice and suffice to convince the board that the appellant has a legitimate interest in the processing of the present case being accelerated before the boards of appeal. The present case has consequently been dealt with by the board considerably out of turn.

3. *The context of the invention*

3.1 The application relates to a processor for executing "Very Long Instruction Words" (VLIW) of a fixed word length, each comprising a number of operation fields

specifying operations for execution in parallel. The terms "instruction" and "operation" are defined on page 12, lines 12 to 21. Claim 1 sets out at least two operation fields. As shown in figure 2A, the 32-bit instruction word stored in the instruction register (10, figure 4) comprises eight 4-bit words, denoted fields P0.0 to P3.2. A decoder unit (20, figure 4) comprises decoders for decoding various fields of the instruction word, as follows.

3.2 As shown in figure 4, the P0.0 field is fed to a format decoder and indicates the instruction type, there being sixteen possible types containing one to three operations; see figures 2B to 2D and page 16, line 7, to page 19, line 7. Some formats contain constants (denoted "const") to be stored in the constant register (36) of the processor; see page 14, lines 14 to 21.

3.3 The P1.0 field (termed the "first type of operation field" in claim 1) is fed to a branch decoder and holds an operation code for a branch instruction, branching controlling the control flow of a program. Thus, as stated on page 4, lines 8 to 11, one operation in the instruction is indicated by an operation code without an explicit indication of an operand. Instead, when the branch instruction is executed, the value stored in the constant register (36) acts as an implicit operand.

3.4 The P2.0 to P2.2 and P3.0 to P3.2 fields (termed the "second type of operation field" in claim 1) each define an operation code and two operands (data source and destination), respectively. The P2.0 and P3.0 fields are fed to first and second operation decoders, respectively.

3.5 The outputs of the instruction register and decoder unit are fed to an execution unit (30), comprising an instruction fetch unit (39). The instruction fetch unit receives an address from the program counter unit (33), shown in figure 7, which can implement branching operations either by adding an offset stored in the constant register to the address value or by using the value in the constant register directly as the target address.

4. *The amendments to the application, Article 123(2) EPC*

4.1 Claim 1 is based on original claims 1 and 6 as well as figures 2a and 4. Page 5, lines 13 to 14, discloses controlling a "control flow" of a program. Claims 2 to 5 are based on figures 2A to 2D and 4. In claims 6, 7 and 8 the addition of the output of branch decoder to the program counter to cause branching is based on page 17, lines 5 to 10, page 20, lines 7 to 9, and page 22, lines 6 to 9. Claims 9 and 10 are based on page 4, lines 8 to 15. Claim 11 is based on page 43, lines 7 to 19.

4.2 Turning to the description, page 2a acknowledges D1 and D2, Rule 27(1)(b) EPC 1973, and page 3 makes a generic reference to claim 1, Rule 27(1)(c) EPC 1973.

4.3 The board is consequently satisfied that the amendments to the application comply with Article 123(2) EPC.

5. *Clarity and support, Article 84 EPC 1973*

5.1 *Support for the expressions in claim 1 "first type of operation field" and "second type of operation field"*

5.1.1 According to the reasons for the appealed decision, regarding a differently worded claim 1, neither the above expressions, now also set out in claim 1, nor the position of these fields in the instruction were defined in the description.

5.1.2 The appellant has responded to this objection by now setting out in claim 1 that the first and second types of operation field are located at first and second predetermined positions in the instruction, respectively. The appellant has also pointed out that the operation fields now set out in claim 1 are supported by original claim 6. As shown in figure 4, the claimed "first type of operation field" is also supported by field P1.0 of the instruction, and the claimed "second type of operation field" is also supported by what is referred to in figure 2A as the "first operation field" 59, namely fields P2.0 to P2.2. Consequently the board finds that the above objections have been overcome.

5.2 *The format field and the corresponding format decoding unit*

5.2.1 According to the reasons for the appealed decision, regarding a differently worded claim 1, the format field P0.0 in the instruction and the corresponding format decoding unit (see figure 4, items 11 and 21) were essential for decoding and executing the

instruction. Hence a claim not setting out these features would not be supported by the description, Article 84 EPC 1973.

5.2.2 Although claim 1 as presently formulated also does not set out a format field or a format decoding unit, the board finds that claim 1 is nevertheless supported by the description, since the invention as summarised from page 3, line 13, to page 4, line 15, does not comprise either the format field or the format decoding unit, neither are they set out in claim 1 as originally filed or shown in figures 12 to 14. The skilled person would also realize that the VLIW processor could use a single one of the possible instruction formats.

5.3 *Instructions with constant data in the operation fields*

5.3.1 According to the reasons for the appealed decision, these "described embodiments" do not fall within the scope of the claims, this inconsistency between the claims and the description rendering the claims unclear.

5.3.2 As present claim 1 sets out the first type of operation field being composed of a control code with no operand thereof and the second type of operation field being composed of an operation code and one or more operands, this claim also does not cover such instructions, for instance instructions type 4 in figure 2C and type B in figure 2D. However this fact is insufficient to make the claims inconsistent with the description and drawings or to render the claims unclear. The board takes the view that it would be unambiguous for the skilled person that such instructions are not intended

to fall within the claims and that the claims are not to be construed in such a way that they do.

5.3.3 Consequently the board finds that the claims satisfy Article 84 EPC 1973.

6. *The prior art*

6.1 *Document D1*

6.1.1 D1 relates to an information processing apparatus having a RISC (Reduced Instruction Set Computing) architecture in which, to simplify and thus speed up the computing hardware, operations are always performed either between registers or between memory and a register. A plurality of operations may also be performed simultaneously; see column 1, lines 15 to 33. In particular, D1 concerns specifying one or more operations in a fixed length "long instruction word". Each "long instruction word" contains an instruction type specifying the structure of the long instruction word and, according to said structure (see the examples in figures 2A to 2D), one or more "instruction words", each specifying an instruction code (OP) and at least one (see column 2, lines 39 to 52) associated operand (Ra, Rb). An operand can either explicitly contain "immediate data" (IMM) or may specify the register containing that data. According to figure 4 and column 7, lines 18 to 37, decoders 25 to 28 decode the type and, according to the type (see column 8, line 47, to column 10, line 7), instruction codes, respectively, whilst further decoders derive their corresponding operands. Thus D1 discloses a decoder unit for decoding the plurality of operation fields in the fetched

instruction in parallel with each other. In view of column 7, lines 11 to 17, D1 also discloses means for fetching an instruction. According to column 12, lines 48 to 52, referring to figure 3, a branch address may be supplied via a latch (61) to the instruction memory (20), so as to read the next long instruction word. According to figure 3 and column 11, lines 30 to 43, said branch address can be derived from the registers specified by operands Rb1 and Rb2 in the long instruction word.

6.1.2 In view of the disclosure in D1 of a branch address being derived from operands Rb1 and Rb2, the board, in contrast to the reasons for the appealed decision, regards fields OPb, Rb1, Rb2, Rb3 as the claimed first type of operation field, and fields OPa, Ra1, Ra2, Ra3 as the claimed second type of operation field.

6.1.3 Hence, in terms of claim 1, D1 discloses: a VLIW processor, comprising: fetch means for fetching an instruction that includes a plurality of operation fields (see figure 2A); and a decoder unit (see figure 4; 25, 26, 27, 28, 24, 31) for decoding the plurality of operation fields in the fetched instruction in parallel with each other, the plurality of operation fields including a first type of operation field (OPb, Rb1, Rb2, Rb3) and a second type of operation field (OPa, Ra1, Ra2, Ra3), the first type of operation field being located at a first predetermined position in the instruction (see figure 2A; "format A", bits 24 to 43), the second type of operation field being located at a second predetermined position in the instruction (see figure 2A; "format A", bits 4 to 23) and is composed of an operation code (OPa) and one or

more operands (Ra1, Ra2, Ra3), the decoder unit including: a first decoder (27) for decoding the control code in the first type of operation field and for controlling a control flow of a program, and a second decoder (26) for decoding the operation code in the second type of operation field.

6.2 *Document D3*

6.2.1 D3 relates to a processing device including a memory circuit and a group of functional units (F). The functional units operate in parallel to execute very long instruction words (VLIW). As shown in figure 1, the memory circuit comprises a plurality of memory units 15, each memory unit comprising two RAM units, each RAM unit storing an operand. The operands are supplied to a corresponding functional unit (F1, F2 ... FN), and the result is fed from the output of said functional unit via a bus system (18) and multiplexing network (22) to the inputs of the memory units. If a functional unit is to read an operand from a RAM unit then the appropriate read address (RA) is provided by the instruction register.

6.2.2 The embodiment shown in figure 2 comprises five functional units, one of which is the branch unit (BR), referred to in the reasons for the appealed decision. The processing device further comprises a sequencer (SEQ) for generating a program counter word (PC) every cycle and an "Instruction Issue Pipeline" (IIP) containing the VLIW program memory which feeds the instruction register (46) with very long instruction words (IW). The instruction words comprise fields for controlling the individual functional units, in

particular the BRC field for controlling the branch unit so as to allow the sequence of instruction addresses generated by the sequencer to be modified to cause branching in the program execution. The BRC field is composed of two 2-bit read addresses, BR.G.RA (guard bit) and BR.A.RA (read address), for selecting the locations of the values of guard bit BR.G and destination address BR.A, respectively, to be read from memory. The branch unit passes the BR.G and BR.A values to the sequencer. If BR.G is true then a branch occurs, the sequencer making the next value of the program counter equal to the destination address BR.A. If however BR.G is false then the sequencer merely increments the program counter.

6.2.3 According to the reasons for the appealed decision, the BRC field contained a 4-bit conditional operation code, but no operand. Instead an implied branch register was used. In particular, BR.G.RA specified a branch condition and BR.A.RA a branch format. The appellant has disputed this argument and, in the board's view, correctly pointed out that the two 2-bit read addresses BR.G.RA and BR.A.RA contained in the BRC field are for selecting one of the four possible locations of the value of the guard bit BR.G and the destination address BR.A, respectively. The board agrees with the appellant that the BR.A.RA field corresponds to an operand used in branching so that, contrary to the reasons for the decision, the branching operation known from D3 does indeed specify an operand.

6.3 *Document D2*

6.3.1 D2 relates to a RISC processor capable of executing instructions of various lengths, indicated by a two-bit length indicator (24); see figure 2. The instructions comprise one or more instruction fields specifying the addresses of sources of data (operands), the operation to perform (opcode; see table B on page 12) and the address of the destination for the result. Not all instructions need specify two source addresses and a destination address, since they are either not required or are implicit. Hence instruction fields can be omitted from an instruction and replaced by a shorter identifier, resulting in a shorter "compressed" instruction. To store the operands and/or result, implicit addressing is implemented using first-in-first-out (FIFO) registers, termed "pipes"; see table A and page 5, lines 1 to 13, and page 9, line 31, to page 10, line 31. For instance, in the case of format 1, shown in table A, a pipe is used both as a source and as a destination address, so that neither address need be specified in the instruction.

6.3.2 The board agrees with the finding in the reasons for the appealed decision that D2 discloses solving the problem of shortening an operation field in an instruction by making an operand implicit, so that its specifier can be removed from the instruction. The board however agrees with the appellant that D2 does not relate specifically to VLIW processors.

7. *Inventive step, Article 56 EPC 1973*

7.1 According to the reasons for the appealed decision, the claimed subject-matter of the fifth auxiliary request (and *obiter* of the fourth auxiliary request) lacked an inventive step in view of the combination of D1 and D3. The decision also stated *obiter dictum* that the claimed subject-matter of the main and first to third auxiliary requests lacked an inventive step in view of the combination of D1 and D2 (where D2 was only used to illustrate a "well known" feature).

7.2 It is common ground between the appellant and the examining division, and the board agrees, that D1 forms the closest prior art. The subject-matter of claim 1 differs from the disclosure of D1 in that the first type of operation field is composed of a control code with no operand thereof.

7.3 The difference feature is known *per se* from D2, in particular format 1 in figure 2, in which no operand is specified because it is implicit that a pipe is to be used both as a source and as a destination. For the reasons given above at point 6.2.3 and contrary to the reasons for the appealed decision, the difference feature is however not known from D3.

7.4 According to the reasons for the appealed decision, the technical effect of the difference feature in a broader form was to shorten the operation field. The problem to be solved was thus how to reduce the length of an operation field, thereby saving memory space. The problem was well known in instruction encoding. A well known solution, as for example known from D2, was to

use implicit operands, whereby operand specifiers were removed from the instruction. The skilled person would therefore have considered this solution as merely one of several straightforward possibilities from which to select "depending on the circumstances", without exercising inventive skill, in order to solve the problem posed. The board points out that this reasoning does not explain which "circumstances" would have led the skilled person to apply the teaching of D2 to D1 in such a way as to arrive at the claimed subject-matter.

7.5 The board is also not convinced that the objective technical problem starting from D1 can be fairly regarded as "to reduce the length of an operation field, thereby saving memory space", as stated in the appealed decision, since this problem is so narrowly formulated as to point to the solution, namely to remove an operand specifier from the instruction word and use an implicit operand instead. Moreover the board is not convinced that reducing the length of an operation field in an instruction field necessarily results in an overall saving of memory. The board takes the view that the objective technical problem starting from D1 can be formulated as to increase code efficiency, this problem being derivable from the application; see page 3, lines 4 to 8.

7.6 The board is not persuaded that the skilled person starting from D1 would have regarded the approach taken in D2 as solving the objective technical problem. Whilst D2 teaches the use of implicit operands in branching instructions, it also teaches that specific additional hardware, namely the first-in-first-out (FIFO) registers, termed "pipes" (see figure 3; pipe

171), must be provided to support the execution of such instructions. The addition of such pipes would however run contrary to the statement in D1 (see column 1, lines 24 to 33) that, according to the RISC approach, it is desirable to simplify the hardware required to execute instructions and also to simplify the control of the hardware, so that the clock frequency can be increased and the number of cycles required to execute an instruction can be reduced. In this context the board finds that it would not have been obvious for the skilled person starting from D1 to have applied the teaching of D2 to arrive at the claimed subject-matter.

7.7 Hence the subject-matter of claim 1 involves an inventive step, Article 56 EPC 1973.

8. *The description*

8.1 Since, in view of the applicant's request received on 25 September 2008 (see point V above) and the amendments to the claims, the description may require adaption, the case is remitted to the first instance, Article 111(1) EPC 1973. This will also allow the first instance to consider whether the expression on page 44, lines 24 to 26, "scope of the present invention", constitutes an unnecessary statement, contrary to Rule 34(1)(c) EPC 1973.

8.2 The board draws the attention of the first instance to the wish of the appellant for accelerated processing of this case before the first instance; see point IV above.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of claims 1 to 11, received on 30 April 2013, drawings sheets 1 to 16, received on 29 September 2006, and a description to be adapted.

The Registrar: The Chairman:

B. Atienza Vivancos D. H. Rees