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Datasheet for the decision of 8 May 2014

Case Number: T 1154/10 - 3.4.03

Application Number: 99927350.1

Publication Number: 1095409

IPC: H01L29/24, H01L29/808, H01L21/04

Language of the proceedings: EN

Title of invention:
SILICON CARBIDE HORIZONTAL CHANNEL BUFFERED GATE SEMICONDUCTOR DEVICES

Applicant:
CREE, INC.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56
EPC Art. 123(2)

Keyword:
Inventive step - (yes)

Decisions cited:

Catchword:

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Case Number: T 1154/10 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 8 May 2014

Appellant: (Applicant)	CREE, INC. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	Boult Wade Tennant Verulam Gardens 70 Gray's Inn Road London WC1X 8BT (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 4 January 2010 refusing European patent application No. 99927350.1 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman:	G. Eliasson
Members:	S. Ward
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 99 927 350 on the grounds that the main request and the first auxiliary request did not fulfill the requirements of Article 123(2) EPC and that the claimed subject-matter of the second auxiliary request did not involve an inventive step within the meaning of Article 56 EPC 1973.

II. At the end of the oral proceedings before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted with the following documents:

Description: pages 1-5, 5A, 5B, 6-20 filed during the oral proceedings before the Board,

Claims: 1-9 filed during the oral proceedings before the Board,

Drawings: Figures 1-5 as published.

All other requests were withdrawn.

III. The following documents cited by the Examining Division are referred to in this decision:

D1: EP 0 703 629 A
D4: US 5 321 283 A

IV. Claim 1 according to the sole request filed in oral proceedings before the Board reads:

"1. A silicon carbide device having a silicon carbide substrate (10) having a first carrier concentration, the device comprising:
a first layer of silicon carbide (12, 12') of a first conductivity type on the silicon carbide substrate (10) and having a carrier concentration less than the first carrier concentration;
a buried region (14, 14') of a second conductivity type semiconductor material in the first layer of silicon carbide (12, 12') that defines a channel region (15) between a first face of the first layer of silicon carbide (12, 12') and the buried region (14, 14');
a first region (18, 18') of semiconductor material of the first conductivity type, doped to a carrier concentration greater than the carrier concentration of the first layer of silicon carbide (12, 12'), wherein the first region (18, 18') of semiconductor material of the first conductivity type is between the buried region of semiconductor material and a face of the first layer of silicon carbide (12, 12') opposite the substrate (10) and adjacent the channel region (15) of the first layer of silicon carbide (12, 12');
a gate layer (16, 16') of semiconductor material of the second conductivity type on the first layer of silicon carbide (12, 12') wherein the gate layer (16, 16') extends to cover the channel region (15) of the first layer of silicon carbide (12, 12');
a gate contact (20) on the gate layer (16, 16') of semiconductor material so as to define the channel region (15) of the first layer of silicon carbide (12, 12');
a first contact (22) on the first region of semiconductor material (18, 18'); and
a second contact (24) on the silicon carbide substrate (10) opposite the first layer of silicon carbide (12, 12');

wherein the thickness and doping of the channel region (15), and the doping of the buried region (14, 14') and the gate layer (16, 16') are such that the channel region is depleted when no bias voltage is applied to the gate contact, and wherein the gate layer is provided with a gate current limiting diode in the form of a layer of highly doped first conductivity type semiconductor material (26, 26') between the gate layer (16, 16') and the gate contact (20)."

V. The appellant's arguments may be briefly summarised as follows:

Claim 1 was essentially based on the second auxiliary request rejected by the Examining Division, but with several amendments, including *inter alia* that "a passage has been added ... to restrict the claim to a normally-off device" and that the claim "has been restricted to the integrated gate current limiting diode." The only contentious issue appeared to be whether or not the subject matter of claim 1 involved an inventive step.

Taking the embodiment of figure 9 of document D1 as the closest prior art, the claimed subject-matter differed in that *inter alia* "a diode, constituted by a layer of highly doped first conductivity type semiconductor material, is disposed between the gate layer and the gate contact of the silicon carbide semiconductor device to limit the gate current of the device".

Contrary to the finding of the Examining Division, there was "nothing in the teaching of D4 which would encourage the skilled person to adopt the diode arrangement disclosed in D4 for use in the JFET of D1 so as to arrive at the subject matter of claim 1".

The problem facing the skilled person starting from D1 was how to limit the gate current, but it must be further specified that this was for a normally-off device, as claimed. The skilled person would not look for a solution to this problem in document D4 which concerned normally-on devices.

Moreover, the relevant embodiment of document D4 (shown in Figure 5A) was of a very different construction to that of the device shown in figure 9 of document D1, and it was unclear how a skilled person would combine these disclosures.

In the claimed normally-off device of the present invention, the gate current limiting diode would be reverse biased when an on-state voltage is applied, whereas in the device shown in document D4 "the second pn junctions (515A, 517A) in the gate regions are not reverse biased when an on-state voltage is applied to the gate." The purpose of this diode was therefore subtly, but significantly different.

Reasons for the Decision

1. The appeal is admissible.

2. Amendments: Article 123(2) EPC

2.1 The subject-matter of claim 1 is directed to a silicon carbide device and can be considered to be based, in

essence, on the subject-matter of claim 1 as originally filed (a silicon carbide channel semiconductor device).

The wording used to describe many of the individual features of the device has been somewhat altered to correspond to the wording used to describe the same features in independent claim 16 as originally filed (directed to a unit cell of a silicon carbide channel transistor) and independent claim 25 as originally filed (directed to a unit cell of a silicon carbide channel thyristor). The Examining Division did not raise any objection under Article 123(2) EPC in this regard, and nor does the Board see any reason to do so.

2.2 The passage on page 13, lines 30-36 is considered to provide an adequate basis - albeit worded slightly differently - for the penultimate feature of the claim ("the thickness and doping of the channel region (15), and the doping of the buried region (14, 14') and the gate layer (16, 16') are such that the channel region is depleted when no bias voltage is applied to the gate contact").

2.3 The final feature of the claim ("the gate layer is provided with a gate current limiting diode in the form of a layer of highly doped first conductivity type semiconductor material (26, 26') between the gate layer (16, 16') and the gate contact (20)") is based on the arrangements depicted in figures 3 and 4 of the application (having particular reference to the layers 26, 26') and the corresponding passages of the description (e.g. page 16, lines 1-7 and 34-36). Claims 3, 17 and 26 as originally filed provide further basis.

The manner in which the gate current limiting diode was claimed in the main and first auxiliary requests on

which the contested decision was based led to the rejection of those requests by the Examining Division under Article 123(2) EPC. However, the objections were directed against the formulation of the first alternative involving a discrete diode; this alternative has been omitted from claim 1 of the present main request.

The present formulation for claiming the gate current limiting diode corresponds essentially to the second alternative of the second auxiliary request on which the contested decision was based, against which no objection was raised under Article 123(2) EPC by the the Examining Division. The Board also sees no reason to raise any objection in this regard.

2.4 Claim 1 also omits the following feature present in claim 1 of the main request as refused: "the gate layer is adjacent but spaced apart from the first region of semiconductor material". Although this feature was present in independent claims 16 and 25 as originally filed, it was not present in the most general originally-filed claim (claim 1), nor is it explained in the application as being essential to the device.

Whilst in the schematic figures 1-4 the gate layer (16, 16') is depicted as being spaced apart from the first (source) region (18, 18'), according to the description (page 12, lines 18-22) the source region (18) may extend under the gate 16 by a distance which "may range from about 0.5 μm to about 3μm", thus apparently disclosing embodiments in which the gate layer and the first region are in contact.

The deletion of a feature which was not comprised in claim 1 as originally filed, is nowhere presented as

essential, and which appears to be inconsistent with disclosed embodiments of the invention is not seen as giving rise to any unallowable extension of subject-matter.

2.5 The dependent claims 2-9 also have an adequate basis in the application as originally filed (see e.g. original claims 4, 9–14, 16 and 25).

2.6 The Board is therefore satisfied that the appellant's request fulfills the requirements of Article 123(2) EPC.

3. Inventive Step

3.1 Closest Prior Art

3.1.1 The Board is of the view that the document D1 – seen by the Examining Division and the appellant as representing the closest prior art – discloses two different types of FET device.

3.1.2 The first type is that disclosed in the figures (1–9) and in the detailed description (column 3, line 8 – column 5, line 19).

This type of device is undoubtedly a "normally-on" FET. This is evident from, for example, figure 8, which shows computer-simulated performance results for the device of figure 2 (see column 3, lines 48–49), in which a maximum drain current density occurs for a gate voltage (Ug) of zero, and the current density decreases as the magnitude of the (negative) gate voltage (Ug) increases. Moreover, the device of figure 2 has a gate of p+ type material forming a pn junction with the channel zone 5, and the negative voltage (see figure 8)

applied to the p+ type base means that the gate-channel junction is operated as a *reverse-biased* pn junction, which is characteristic of a depletion-mode (normally-on) device.

Figure 9 shows an alternative manner of implementing the device of figure 1 ("*eine alternative Ausführungsform des Bauelements nach Fig. 1*" - see column 3, lines 5-6). The Board agrees with the view of the Examining Division that this modification is to be understood "in conjunction with the simpler devices of figures 1 and 2". The device of figure 9 is therefore also seen as a normally-on device.

3.1.3 A second type of device is described briefly in column 2, point 4, and is explicitly described as "normally-off". This arrangement is said to be possible since the height of the epitaxial layer (i.e. the channel region) can we varied at will. It is implicit that this device will also incorporate those features described as essential to the invention, in particular in column 2, lines 2-18 ("*Das Wesen der Erfindung besteht darin ...*"). Document D1 does not, however, disclose a normally-off device having the precise structure shown in figure 9, and in particular it does not disclose a normally-off device having a gate structure in the form of a pn junction, a feature which is only disclosed in connection with normally-on variants.

3.1.4 A decision on inventive step was only taken by the Examining Division in relation to the second auxiliary request, claim 1 of which was not limited to either normally-off or normally-on devices, but covered both. The Examining Division selected - reasonably, in the opinion of the Board - the normally-on device of figure 9 as the closest prior art.

However, claim 1 of the present main request comprises the following feature:

- *"the thickness and doping of the channel region (15), and the doping of the buried region (14, 14') and the gate layer (16, 16') are such that the channel region is depleted when no bias voltage is applied to the gate contact"*.

Hence, the claimed subject-matter is now restricted to normally-off devices.

Although both normally-off and normally-on devices are well-known, they represent two distinct classes in FET technology. While the device of figure 9 of document D1 might well represent a plausible starting point for developing an improved normally-on device, in the opinion of the Board it represents an inherently unlikely choice where the claimed invention is a device of a different type - i.e. normally-off (see "Case Law of the Boards of Appeal of the EPO", 7th ed. 2013, I.D.3.4.3).

3.1.5 The Board therefore considers that the closest prior art is the second type of device referred to under point 3.1.3, above, which is explicitly described as "normally-off", and in relation to which no particular type of gate arrangement is disclosed.

3.2 Difference, Problem and Solution

3.2.1 The subject-matter of claim 1 differs from the closest prior art at least in the provision of the following two features (reference signs omitted):

(a) *"a gate layer of semiconductor material of the second conductivity type on the first layer of silicon carbide wherein the gate layer extends to cover the channel region of the first layer of silicon carbide"*; and

(b) "the gate layer is provided with a gate current limiting diode in the form of a layer of highly doped first conductivity type semiconductor material between the gate layer and the gate contact."

3.2.2 In order to formulate the objective problem it is therefore necessary to identify the specific technical effects and advantages described in the application as being provided by the features (a) and (b).

Normally-off (enhancement-mode) devices may conventionally be constructed using MOSFET technology. However, several disadvantages associated with MOSFET arrangements are described in the application as filed (page 3, line 3 - page 4, line 33), in particular gate oxide degradation by Fowler-Nordheim (F-N) current. The choice of a semiconductor gate layer (feature (a)) is described as advantageous in eliminating the F-N current problem (page 5, line 37 - page 6, line 14 of the application as filed).

The advantage of feature (b) is described as being to limit the gate current (see, for example, page 7, lines 1-11 of the application as filed).

3.2.3 Two problems can therefore be identified: a first problem solved by feature (a) of avoiding gate degradation by Fowler-Nordheim current, and a second

problem solved by feature (b) of limiting the gate current (in the claimed normally-off device).

3.2.4 In relation to the first problem, clearly one obvious solution to preventing gate damage by Fowler-Nordheim current would be to avoid the MOS arrangements in which this effect arises.

Document D1 describes (in the context of the device of figure 9 – see column 4, lines 20–24) the two most commonly used gate structures in FET technology: a semiconductor layer such that the gate/channel interface forms a pn junction, and a metal oxide semiconductor (MOS) arrangement. Consequently, in seeking to avoid the problems inherent in MOS gate structures, it would be obvious for the skilled person to opt for the other type of gate structure disclosed in document D1, namely a pn junction.

Whether it would also be obvious to select the particular pn junction gate arrangement of feature (a) – an arrangement broadly corresponding to that of figure 9 of document D1 – rather than some other pn junction gate arrangement (for example, that of figures 1 and 2) is open to question.

3.2.5 However, it is not considered necessary to decide on this matter, since, for the reasons set out below, the Board takes the view that even if it is assumed *arguendo* that feature (a) is an obvious solution to the first problem, it would not be obvious to a skilled person to arrive at feature (b) as a solution to the second problem mentioned above.

3.2.6 In the contested decision, the document D4 was cited as providing a solution to the problem of limiting the

gate current. Document D4 discloses high power (column 1, lines 6-10) JFET arrangements of the normally-on type (column 2, lines 12-13). In column 10, lines 55-65, a problem is identified in relation to the prior art JFET of figure 1 in that "the gate-to-source junction may become forward biased when the source input signal increases above a certain threshold or power level" in which case JFET 100 would be overdriven and "may be destroyed by excess current."

The proposed solution (see column 9, line 61 to column 11, line 28 and figures 5A to 5D) is to provide a layer of highly doped first conductivity type semiconductor material (regions 515, 517 of type N+) between the gate layer (pockets 503, 504 of type P+) and the gate contact (gate electrodes 510, 512), thereby forming second pn junctions 515A, 517A. In effect, the gate is provided with back to back diodes such that one of the diodes is always reversed biased (column 11, lines 10-12 and figure 5B), thereby preventing excess gate current.

3.2.7 The Board therefore accepts that according to document D4 the problem of excessive gate current is solved by providing an additional semiconductor layer between the gate layer and the gate contact to form a gate current limiting diode, and that this also corresponds to the solution according to claim 1 of the present invention.

It must be recalled, however, that the starting point for the present discussion is the *normally-off* device disclosed in document D1 (column 2, point 4). The question is therefore whether it would be obvious to the skilled person to modify such an arrangement by adopting the solution to the problem of excessive gate current disclosed in document D4.

3.2.8 When the device of document D4 is operating normally (i.e. it is not being "overdriven"), the gate junction is reverse-biased and the second pn junction is forward-biased (the majority of the applied voltage being dropped across the reverse biased gate-channel junction). In a normally-off device, on the other hand, in the on-state the gate junction is forward-biased, and a corresponding second pn junction would be reverse-biased (the applied voltage being dropped over both the reverse biased second pn junction diode and the channel depletion layer).

Furthermore, in the arrangement of D4, the second pn junction protects the device from excessive gate current arising in the abnormal and undesirable case that an excessive signal puts the gate-channel junction into forward bias. By contrast, in a normally-off device, the gate-channel junction is intentionally forward-biased in normal operation.

In the light of such considerations, it would not be obvious to the skilled person that the means disclosed in document D4 for preventing excessive gate current in a normally-on device would be similarly effective in solving the same problem in a normally-off device.

3.2.9 According to the description of the present application (page 14, lines 3-13), the manner in which a gate current limiting diode prevents excessive gate current in a *normally-off* device is essentially as follows:

If (in the absence of a gate current limiting diode) the forward biased voltage which is applied to the gate under normal driving conditions is increased to the point where it exceeds the built-in voltage of the

gate-channel pn junction, an excess gate current may arise. This is prevented by providing an additional semiconductor layer between the gate layer and the gate contact to form a diode which is always reverse biased.

Hence, the additional semiconductor layer of the present invention provides a gate current limiting effect in the case of a normally-off device, but in different way from that disclosed in document D4.

3.2.10 The argument that the subject-matter of claim 1 is obvious on the basis of the combination of documents D1 and D4 relies *inter alia* on the hypothesis that a skilled person seeking a solution to the problem of excessive gate current in a normally-off device would look to document D4, which deals only with normally-on devices. The plausibility of this assumption is already questionable.

Moreover, it would be necessary for the skilled person to realise that the additional semiconductor layer proposed in relation to a normally-on device in document D4 could still provide a gate current limiting effect in a normally-off device, albeit in a way which is different to that disclosed in document D4.

In the view of the Board, to arrive at this insight would require the sort of imaginative thinking which is beyond the capacity of the notional skilled person.

3.3 Hence, for the above reasons, the Board judges that the subject-matter of claim 1 involves an inventive step within the meaning of Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent with the following documents:

   Description: pages 1-5, 5A, 5B, 6-20 filed during the oral proceedings before the Board,

   Claims: 1-9 filed during the oral proceedings before the Board,

   Drawings: Figures 1-5 as published.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated