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Datasheet for the decision of 6 May 2014

Case Number: T 1082/10 - 3.4.03

Application Number: 01998081.2

Publication Number: 1374300

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Language of the proceedings: EN

Title of invention:
DAMASCENE PROCESSING USING DIELECTRIC BARRIER FILMS

Applicant:
ADVANCED MICRO DEVICES, INC.

Headword:

Relevant legal provisions:
EPC Art. 123(2)
EPC 1973 Art. 84, 56

Keyword:
Added subject-matter (no)
Clarity, support by description (no)
Inventive step (no)

Decisions cited:

Catchword:

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Case Number: T 1082/10 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 6 May 2014

Appellant: (Applicant)	ADVANCED MICRO DEVICES, INC. One AMD Place Mail Stop 68 P.O. Box 3453 Sunnyvale CA 94088-3453 (US)
Representative:	Eve, Rosemary Margaret Brookes Batchellor LLP 46 Chancery Lane London WC2A 1JE (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 22 December 2009 refusing European patent application No. 01998081.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman:	G. Eliasson
Members:	R. Bekkering
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the refusal of application no. 01 998 081 for added subject-matter, Article 123(2) EPC (main and first auxiliary request) and for lack of clarity, Article 84 EPC, and for added subject-matter, Article 123(2) EPC (second auxiliary request).

II. With the statement setting out the grounds of appeal dated 22 April 2010, the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following:

Main request:

Claims 1 to 14 according to the main request filed with the statement setting out the grounds of appeal,

Auxiliary request:

Claims 1 to 14 according to the auxiliary request filed with the statement setting out the grounds of appeal.

III. A summons to oral proceedings was issued by the board, provided with an annex in which a provisional opinion of the board on the matter was given.

In particular, the appellant was informed that claim 1 of the main request lacked clarity and support by the description, Article 84 EPC 1973, and lack of an inventive step in the sense of Article 56 EPC 1973 over document

D3: EP 0 892 428 A.

The same applied to claim 1 of the auxiliary request.

No arguments were provided by the appellant in response to the board's observations. The board was informed that the appellant would not attend the oral proceedings.

Oral proceedings were held in the absence of the appellant.

IV. Claim 1 of the main request reads as follows:

"*A method of manufacturing a semiconductor device, the method comprising:*
forming a first dielectric layer (30) overlying a substrate (10);
forming a first diffusion barrier layer (31), comprising a first dielectric barrier material, directly on the first dielectric layer;
etching by a first etching process to form a first opening (32) entirely within and defined by side surfaces (30A) of the first dielectric layer and a bottom over an underlying conductive feature;
forming a second diffusion barrier layer (40), comprising a second dielectric barrier material different from the first dielectric barrier material, on and in contact with an entire upper surface of the first diffusion barrier layer overlying the first dielectric layer, on the side surfaces of the first dielectric layer defining the first opening and on the bottom of the first opening;
etching by a second etching process in which said first diffusion barrier layer acts as an etch stop layer to remove the second diffusion barrier layer from, and stopping on, the upper surface of the first diffusion barrier layer, and to remove the second diffusion

barrier layer from the bottom of the first opening exposing the underlying conductive feature, leaving a portion of the second diffusion barrier layer as a liner (50) on the side surfaces of the first dielectric layer defining the first opening (32);
filling the first opening with metal,
forming an overburden on the first barrier layer,
planarizing to form a lower metal feature (60)
forming a third diffusion barrier layer (70), comprising a third dielectric barrier material different from the first dielectric barrier material, on the first diffusion barrier layer and on an upper surface of the lower metal feature;
forming a second dielectric layer (71) on the third diffusion barrier layer;
forming a fourth diffusion barrier layer (72), comprising a fourth dielectric barrier material, on the second dielectric layer;
etching to form a second opening (75) entirely within and defined by side surfaces (71A) of the second dielectric layer and a bottom over the lower metal feature (60):
whereby even if the second opening is misaligned with the lower metal feature such that the bottom of the second opening is formed partly on the upper surface of the first diffusion barrier layer (31), the second dielectric layer is protected from the lower metal feature by the third diffusion barrier layer (70)."

V. Claim 1 of the auxiliary request corresponds to claim 1 of the main request with the expression "*diffusion barrier layer*" being replaced by "*barrier layer*".

VI. The appellant submitted with the statement setting out the grounds of appeal in substance the following arguments:

Contrary to what was held in the decision under appeal, it was entirely clear that the barrier layers were diffusion barrier layers. The specification (page 1, final paragraph and page 2) stated that "*however, due to copper diffusion through dielectric materials ... copper interconnect structures must be encapsulated by diffusion barrier layer ... the use of such barrier materials to encapsulate copper is not limited to the interface between copper ...*". This indicated to a skilled reader that the barrier layers referred to through the specification and in particular in the claims, were clearly provided to prevent copper or other metal diffusion.

Furthermore, in the introduction, there was reference in the third paragraph of page 2 to problems where feature sizes were reduced with electromigration and capacitance. In particular, it was difficult to accommodate misalignment problems in multilevel interconnection technology. Claim 1, and in particular the last few paragraphs of claim 1, dealt with this problem.

Reasons for the Decision

1. The appeal is admissible.

2. Main request

2.1 *Clarity, support by the description*

According to the application, "*due to Cu diffusion through dielectric materials, such as silicon dioxide, Cu interconnect structures must be encapsulated by a diffusion barrier layer*" (page 1, lines 35 to 36) and "*the use of a conventional metallic barrier film* [...] *becomes problematic in various respects*" (page 2, lines 11 to 12). The objectives of the application are achieved "*by the strategic use of a dielectric barrier layer in lieu of a metal-containing or metallic barrier layer*" (page 3, lines 29 to 30). Moreover, "*Barrier layer 40 comprises a dielectric material different from the dielectric material of barrier layer 31, such that barrier layer 31 functions as an etch stop layer during subsequent etching*" (page 5, lines 8 to 10).

Accordingly, it is considered essential to the performance of the invention that the first to fourth barrier layers provide a barrier against diffusion of Cu (or other metal) of the interconnect structure and consist of (rather than merely comprise) a dielectric material, and that the dielectric material of the second barrier layer is different from the dielectric material of the first barrier layer, such that the first barrier layer functions as an etch stop layer when etching the second barrier layer.

It is noted that, contrary to what is held in the decision under appeal, the application as originally filed is considered to provide a basis for these features within the meaning of Article 123(2) EPC.

However, as claim 1 does not clearly define all of the above essential features of the invention, it lacks clarity and support by the description, contrary to the requirements of Article 84 EPC 1973.

The above was noted in the annex to the summons to oral proceedings. No arguments were submitted by the appellant in response.

2.2 *Novelty*

2.1.1 Document D3

Document D3 discloses a method of manufacturing a semiconductor device (cf column 10, line 36 to column 12, line 55; figures 12 to 18).

The method comprises, using the terminology of claim 1:
forming a first dielectric layer (166) overlying a substrate;
forming a first diffusion barrier layer (178), comprising a first dielectric barrier material, directly on the first dielectric layer;
etching by a first etching process to form a first opening (180) entirely within and defined by side surfaces of the first dielectric layer and a bottom over an underlying conductive feature (162);
forming a second diffusion barrier layer (186), comprising a second dielectric barrier material, on and in contact with an entire upper surface of the first diffusion barrier layer overlying the first dielectric layer, on the side surfaces of the first dielectric layer defining the first opening and on the bottom of the first opening;
etching by a second etching process in which said first diffusion barrier layer acts as an etch stop layer to remove the second diffusion barrier layer from, and stopping on, the upper surface of the first diffusion barrier layer, and to remove the second diffusion barrier layer from the bottom of the first opening exposing the underlying conductive feature, leaving a

portion of the second diffusion barrier layer as a liner on the side surfaces of the first dielectric layer defining the first opening;
filling the first opening with metal (188),
forming an overburden on the first barrier layer,
planarizing to form a lower metal feature (188)
forming a third diffusion barrier layer (190), on the first diffusion barrier layer (178) and on an upper surface of the lower metal feature (188);
forming a second dielectric layer (192) on the third diffusion barrier layer (190);
forming a fourth diffusion barrier layer (212) on the second dielectric layer (192);
etching to form a second opening (200) entirely within and defined by side surfaces of the second dielectric layer and a bottom over the lower metal feature (188);
whereby even if the second opening is misaligned with the lower metal feature such that the bottom of the second opening (200) is formed partly on the upper surface of the first diffusion barrier layer (178), the second dielectric layer (192) is protected from the lower metal feature (188) by the third diffusion barrier layer (190).

In particular, it is noted that according to D3 the (third) barrier layer 186 (second diffusion barrier layer in claim 1) may be of a non-conductive material (column 12, lines 45 to 49). Furthermore, the first diffusion barrier layer (178) need not be removed in the planarizing step (column 11, lines 55 to 57).

Not disclosed in D3 is that:

- the second and third dielectric barrier materials are different from the first dielectric barrier material, and

- the fourth diffusion barrier layer comprises a dielectric barrier material.

Accordingly, the subject-matter of claim 1 of the main request is new over document D3, Article 54(1) EPC 1973.

2.1.2 The subject-matter of claim 1 of the main request is also new over the remaining available, more remote prior art.

2.2 Inventive step

2.2.1 The two distinguishing features above do not achieve a technical effect in combination. Rather, partial problems are independently solved by each of the distinguishing features.

Regarding the above first distinguishing feature, as would be readily apparent to a skilled person, and is indicated in the application for the second diffusion barrier layer (page 5, lines 8 to 10), the effect of this feature is that the first diffusion barrier layer acts as an etch stop layer when etching the second and third diffusion barrier layer, respectively.

The objective, partial problem to be solved relative to D3 may thus be formulated as how to selectively remove the second and third diffusion barrier layers from the underlying first diffusion barrier layer.

Regarding the above second distinguishing feature, the objective, partial problem to be solved relative to D3 is to select an appropriate barrier material for the fourth diffusion barrier layer.

As far as the above first partial problem is concerned, in the method of D3, both the second and third diffusion barrier layers (186, 190) are to be removed without removing the underlying first diffusion barrier layer (178). For a person skilled in the art, familiar with etch processes, it would be obvious to achieve this by selecting different materials for the respective layers.

Regarding the above second partial problem, it would be obvious to the skilled person to select a dielectric material for the fourth diffusion barrier layer, as conductivity is not desirable for this layer.

The above was noted in the annex to the summons to oral proceedings. The appellant did not submit any arguments in response.

2.2.2 In the statement setting out the grounds of appeal the appellant argued that claim 1, and in particular the last few paragraphs of claim 1, dealt with misalignment problems in multilevel interconnection technology.

However, as noted above, in document D3, like in the application, if the second opening (200) is misaligned with the lower metal feature (188) such that the bottom of the second opening (200) is formed partly on the upper surface of the first diffusion barrier layer (178), the second dielectric layer (192) is protected from the lower metal feature (188) by the third diffusion barrier layer (190) (cf figures 17, 18 and corresponding description). Accordingly, D3 too deals with the problem of misalignment in multilevel interconnection technology.

2.2.3 Accordingly, the subject-matter of claim 1 of the main request is obvious to a person skilled in the art and, thus, lacks an inventive step in the sense of Article 56 EPC 1973.

The appellant's main request is, therefore, not allowable.

3. *Auxiliary request*

Claim 1 of the auxiliary request only differs from claim 1 of the main request in that the expression "*diffusion barrier layer*" is replaced by "*barrier layer*".

This amendment does, however, not alter the findings above for the main request.

In fact, as noted above, it is essential to the performance of the invention that the first to fourth barrier layers provide a barrier against diffusion of Cu (or other metal) of the interconnect structure.

Accordingly, for the same reasons given above for claim 1 of the main request, claim 1 of the auxiliary request lacks clarity and support by the description, contrary to the requirements of Article 84 EPC 1973.

Moreover, for the same reasons given above for claim 1 of the main request, the subject-matter of claim 1 of the auxiliary request lacks an inventive step in the sense of Article 56 EPC 1973.

Also for the auxiliary request, no arguments were submitted by the appellant in response to the board's observations provided in the annex to the summons to oral proceedings, which correspond to the above.

Accordingly, the appellant's auxiliary request is not allowable either.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:	The Chairman:

S. Sánchez Chiquero	G. Eliasson

Decision electronically authenticated