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Datasheet for the decision of 7 October 2015

Case Number: T 0724/10 - 3.5.01

02000378.6 Application Number:

Publication Number: 1197830

IPC: G06F13/16, G11C8/04, G11C11/401

Language of the proceedings: ΕN

Title of invention:

Integrated circuit I/O using a high performance bus interface

Patent Proprietor:

Rambus Inc.

Opponents:

MICRON EUROPE Ltd SK hynix Deutschland GmbH

Headword:

Synchronous DRAM device/RAMBUS

Relevant legal provisions:

EPC Art. 113(2) EPC R. 103(1)(a)RPBA Art. 11

Keyword:

Substantial procedural violation - (yes) Basis of decision - text submitted or agreed by applicant (no) Reimbursement of appeal fee - (yes) Remittal to the department of first instance - (yes)

Decisions cited:

T 0543/92, T 0089/94, T 0647/93

Catchword:



Beschwerdekammern Boards of Appeal Chambres de recours

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Case Number: T 0724/10 - 3.5.01

DECISION of Technical Board of Appeal 3.5.01 of 7 October 2015

Appellant: Rambus Inc.

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Representative: Eisenführ Speiser

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Respondent: MICRON EUROPE Ltd

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Respondent: SK hynix Deutschland GmbH

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Decision under appeal: Decision of the Opposition Division of the

European Patent Office posted on 8 March 2010 revoking European patent No. 1197830 pursuant to

Article 101(3)(b) EPC.

Composition of the Board:

Chairman R.R.K. Zimmermann Members: P. Scriven

I. Beckedorf

- 1 - T 0724/10

Summary of Facts and Submissions

- I. The patent proprietor (hereinafter: the appellant) appeals the opposition division's decision, dated 8 March 2010, to revoke European patent No. EP 1 197 830.
- II. The patent originates from European patent application EP02000378.6, a divisional of the earlier application EP99118308.8 (the "parent application"). The parent application is, in turn, a divisional application originating from the application EP919083741.1 (the "root application"), published as WO 91/16680 A1.
- III. The opposition division revoked the patent on the ground that the subject-matter of "all requests" extended beyond the content of the root application as filed (Article 100(c) EPC).
- IV. The requests at the start of the oral proceedings lasting two days (from 8 to 9 December 2009) were a main request and four auxiliary requests (I to IV) filed with letter dated 5 November 2009.
- V. On the first day of oral proceedings , the proprietor filed amended auxiliary requests I and II; the previous auxiliary requests I to IV were maintained and renumbered as auxiliary requests III to VI.
- VI. On the second day of the oral proceedings, the proprietor submitted a new version of auxiliary request I, replacing both auxiliary requests I and II filed the day before. The other auxiliary request were again renumbered, this time as auxiliary requests II to V. At the end of the oral proceedings, the requests were,

- 2 - T 0724/10

thus, as follows:

- the main request of 5 November 2009;
- auxiliary request I of 9 December 2009;
- auxiliary requests II to V corresponding to auxiliary requests I to IV of 5 November 2009.
- VII. The appellant requested that the decision under appeal be set aside and that the patent be maintained on the basis of the main request of 5 November 2009 or one of the following auxiliary requests:

 auxiliary request I of 9 December 2009;

 auxiliary requests II to III of 5 November 2009;

 auxiliary request IV to VII as filed with the statement setting out the grounds of appeal.

The appellant also requested the reimbursement of the appeal fee on the ground of a substantial procedural violation (Rule 103(1)(a) EPC), and oral proceedings as an auxiliary request.

The appellant's arguments, in so far they are relevant to the present decision, can be summarized as follows:

In its decision, the opposition division did not give reasons why auxiliary request I, as filed on the second day of the oral proceedings, contravened Article 100(c) EPC. Instead, the decision dealt with the withdrawn auxiliary requests I and II, filed on the first day of the oral proceedings. Ignoring the proprietor's amended requests was a substantial procedural violation according to T 543/92 and T 89/94.

VIII. Opponent I replied that it had nothing to add beyond the arguments made during the first instance procedure.

- 3 - T 0724/10

It subsequently withdrew its opposition to the patent.

Opponent II responded to the statement of grounds that, while it was apparent that the written decision dealt with the wrong version of auxiliary requests I and II, the proprietor was not adversely affected. All requests were extensively discussed during the oral proceedings, and it was clear that they all had the same problem in the "opcode" feature.

Opponent II has also withdrawn its opposition to the patent.

IX. Claim 1 of the main request reads:

"A synchronous Dynamic Random Access Memory (DRAM) semiconductor device including a memory array having a plurality of dynamic memory cells, wherein the memory device comprises:

connection means adapted to connect the DRAM to an external bus which is a part of a semiconductor bus architecture, the semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to the external bus, wherein the external bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the DRAM for communication with substantially every other semiconductor device connected to the external bus, the connection means being adapted to receive multiplexed addresses;

clock receiver circuitry to receive an external
clock signal;

a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal (53, 54) to transpire after which the DRAM responds to an operation

- 4 - T 0724/10

code, the programmable access-time register being accessible to the external bus through the connection means, wherein to set the value in the programmable access-time register data is transmitted to the programmable access-time register over the external bus;

sense amplifiers, coupled to the memory array, to sense data from the dynamic memory cells;

a plurality of input receivers to sample the operation code synchronously with respect to a first transition of the external clock signal, wherein the operation code instructs the memory device to:

perform a read operation such that the memory device outputs the data sensed by the sense amplifiers; and

precharge the sense amplifiers automatically
after the data is sensed;

and

a plurality of output drivers (76) for outputting the data onto the external bus (18, 65) in response to the operation code, wherein the output drivers (76) output the data on the external bus (18, 65) after the number of clock cycles of the external clock signal transpire and synchronously with respect to the external clock signal (53, 54), so that receipt of the operation code and the corresponding response are separated by the number of clock cycles as selected by the value stored in the programmable access-time register, wherein each output driver of the plurality of output drivers (76) outputs the data onto the external bus (18, 65) at a bus cycle data rate that is twice the rate of the external clock signal."

X. According to a handwritten annex to the minutes of oral proceedings, auxiliary request I, as filed on the first - 5 - T 0724/10

day of the oral proceedings, included the following text:

"wherein, when the operation code is part of a request packet consisting of a contiguous series of bytes, the access time is also representative of a time between receipt of the request packet and the corresponding response."

XI. Claim 1 of auxiliary request I, as filed on the second day of the oral proceedings, differs from claim 1 of the main request by the addition of the following feature after the word "access-time register" at the third line from the end:

"wherein the value stored in the register is also representative of an amount of time between receipt of all information required to enable the DRAM to respond to the operation code and the corresponding response,"

XII. Auxiliary request II filed as on the first day of the oral proceedings includes the following text:

"wherein, when the operation code is part of a request packet consisting of a contiguous series of bytes, the value stored in the register is also representative of a time between receipt of the request packet and the corresponding response,

wherein, when the operation code is not part a request packet, the value stored in the register is also representative of a time between receipt of all information required to enable the memory device to respond to the operation code and the corresponding response."

- 6 - T 0724/10

Reasons for the Decision

- 1. Substantial procedural violation
- 1.1 According to Article 113(2) EPC, the EPO shall examine, and decide upon, the European patent application or the European patent only in the text submitted to it, or agreed, by the applicant or the proprietor of the patent.
- 1.2 The decision of the opposition division does not explicitly define the requests on which it is based. However, in section 3.4, reference is made to the feature:

"wherein when the operation code is part of a request packet consisting of a contiguous serious of bytes, the access time is also representative of a time between receipt of the request and the corresponding response"

This feature is defined in claim 1 according to the version of auxiliary request I filed on the first day of the oral proceedings, but not in the version filed on the second day. Furthermore, the decision mentions no feature present in the request filed on the second day, but not in the in the request filed on the first day.

Similarly, section 3.5 recites the feature:

"wherein, when the operation code is part of a request packet consisting of a contiguous series of bytes, the the value stored in the register is also representative - 7 - T 0724/10

of a time between receipt of the request and the corresponding response,

wherein, when the operation code is not part of a request packet, the value stored in the register is also representative of a time between receipt of all information required to enable the memory device to respond to the operation code and the corresponding response".

This feature is defined in claim 1 according to auxiliary request II, filed on the first day of the oral proceedings and withdrawn on the second day, but not in the auxiliary request that was renumbered as auxiliary request II during the second day.

- 1.3 The Board cannot conclude that this was a mere mistake in the written decision, but considers that the decision to revoke the patent was taken on a version of the claims no longer maintained by the appellant in violation of Article 113(2) EPC.
- Opponent II argued that the proprietor was not adversely affected by this. The Board disagrees. Enshrined in Article 113(2) EPC is the principle of party disposition. It gives the patent applicant, or patent proprietor, the right to dispose of its requests as it sees fit, and, thereby, the right to control the subject-matter forming the basis of the procedure. This is a procedural right of such fundamental importance that any infringement of it must, in principle, be considered as a substantial procedural violation (T 647/93, OJ EPO 1995, 132).
- 1.5 In view of the substantial procedural violation in the first instance proceedings, the Board sees no other

Т 0724/10

option than to remit the case to the first instance for consideration of the requests put forward by the proprietor (Article 111(1) EPC; Article 11 RPBA). The Board considers reimbursement of the appeal fee to be equitable in the present circumstances (Rule 103(1)(a) EPC). The Board remits the case because of a fundamental deficiency (serious procedural flaw). This should not be understood as reflecting disapproval, or indeed approval, of the opposition division's substantive reasoning. The Board refrains from making any comment on the matter.

- 8 -

Order

For these reasons it is decided that:

- 1. The case is remitted to the opposition division for further prosecution.
- 2. The appeal fee is to be reimbursed.

The Registrar:

The Chairman:



T. Buschek

R.R.K. Zimmermann

Decision electronically authenticated