

**Internal distribution code:**

- (A) [ - ] Publication in OJ  
(B) [ - ] To Chairmen and Members  
(C) [ - ] To Chairmen  
(D) [ X ] No distribution

**Datasheet for the decision  
of 27 May 2014**

**Case Number:** T 0615/10 - 3.5.02

**Application Number:** 04751641.4

**Publication Number:** 1639710

**IPC:** H03M1/10

**Language of the proceedings:** EN

**Title of invention:**  
Analog to digital converter

**Applicant:**  
Netlogic Microsystems, Inc.

**Headword:**

**Relevant legal provisions:**  
EPC Art. 56

**Keyword:**  
Inventive step - (no)

**Decisions cited:**

**Catchword:**



**Beschwerdekammern  
Boards of Appeal  
Chambres de recours**

European Patent Office  
D-80298 MUNICH  
GERMANY  
Tel. +49 (0) 89 2399-0  
Fax +49 (0) 89 2399-4465

Case Number: T 0615/10 - 3.5.02

**D E C I S I O N  
of Technical Board of Appeal 3.5.02  
of 27 May 2014**

**Appellant:** Netlogic Microsystems, Inc.  
(Applicant) 3975 Freedom Circle, Suite 900  
Santa Clara, CA 95054 (US)

**Representative:** Bosch, Matthias  
Bosch Jehle  
Patentanwaltsgesellschaft mbH  
Flüggenstrasse 13  
80639 München (DE)

**Decision under appeal:** **Decision of the Examining Division of the European Patent Office posted on 10 November 2009 refusing European patent application No. 04751641.4 pursuant to Article 97(2) EPC.**

**Composition of the Board:**

**Chairman** M. Ruggiu  
**Members:** M. Léouffre  
P. Mühlens

## Summary of Facts and Submissions

- I. The applicant appealed against the decision of the examining division, posted on 10 November 2009, to refuse the application No.04751641.4. The appeal was received on 6 January 2010.
- II. The reason given in the decision under appeal was that the subject-matter of claim 1 did not involve an inventive step in the sense of Article 56 EPC. The division referred in particular to the following prior art documents:
- D1 : FRANK W.: "Compensation of Linear and Nonlinear Sensor Distortions by Digital Post Processing", SENSOR PROCEEDINGS INTERNATIONAL CONFERENCE FOR SENSORS TRANSDUCERS AND SYSTEMS, 1995, pages 889 to 892 (XP002363900).
  - D2 : EP 0 964 524 A2, and
  - D3 : SUNG-UNG KWAK & al "A 15-b, 5-Msample/s Low-Spurious CMOS ADC" IEEE Journal of Solid-State Circuits, Vol. 32, No. 12, December 1997 (XP011060625).
- III. With the statement of grounds of appeal, received on 16 March 2010, the appellant filed a new main request and three auxiliary requests.
- IV. The board issued a communication together with the summons to attend oral proceedings in which it discussed the clarity of the claims and questions of inventive step having regards to documents D2, D1 and D3.
- V. Oral proceedings took place as scheduled on 27 May 2014, in the absence of the appellant.

VI. With the statement of grounds of appeal the appellant had requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 11 of the main request, or on the basis of the claims of one of the auxiliary requests 1 to 3, all filed with letter dated 16 March 2010.

VII. Claim 1 of the main request reads as follows:

"A method of correcting for output distortion of an analog to digital converter, comprising:  
receiving an output of the analog to digital converter at a calibration module;  
training the calibration module adaptively to estimate the output distortion and obtain an estimated distortion of an output of the analog to digital converter, wherein:  
the output includes a plurality of output bits;  
the plurality of output bits include a plurality of higher order bits and at least one lower order bit that is separate from the plurality of higher order bits;  
the estimation is based at least in part on a function of the plurality of higher order bits of the output;  
feeding forward the estimated distortion of the output of the analog to digital converter to a combiner;  
combining the output of the analog to digital converter with the estimated distortion of the output of the analog to digital converter to compensate for the output distortion; and  
wherein the calibration module comprises a nonlinear filter; and wherein the nonlinear filter includes at least one linear filter coupled with at least one nonlinear element."

Claims 2 to 9 are dependent on claim 1.

Claim 10 of the main request reads as follows:

"A compensating device for correcting output distortion of an analog to digital converter, comprising:  
a calibration device that is arranged to receive an output of the analog to digital converter and adaptively trained to estimate the output distortion of an output of the analog to digital converter and generate an estimated distortion, wherein:  
the output includes a plurality of output bits;  
the plurality of output bits include a plurality of higher order bits and at least one lower order bit that is separate from the plurality of higher order bits;  
the estimation is based at least in part on a function of the plurality of higher order bits of the output;  
a combiner configured to combine the output of the analog to digital converter with the estimated distortion of the output of the analog to digital converter, said estimated distortion fed forward from the calibration module to compensate the output distortion; and  
wherein the nonlinear filter includes at least one linear filter coupled with at least one nonlinear element."

Claim 11 is dependent on claim 10.

VIII. Claim 1 of the first auxiliary request reads as follows:

"A method of correcting for output distortion of an analog to digital converter, comprising:  
in a first state, adaptively training a calibration module; including:  
sending a training signal to the calibration module;  
and

adapting a configuration of the calibration module to reduce a difference between a distortion signal and a simulated distortion signal;  
in a second state, performing distortion correction, including:  
disconnecting an adaptation path in the calibration module;  
modeling distortion of the analog to digital converter using the configuration of the calibration module obtained during the first state;  
generating an estimated distortion of the output of the analog to digital converter;  
feeding forward the estimated distortion of the output of the analog to digital converter to a combiner; and  
combining the output of the analog to digital converter with the estimated distortion of the output of the analog to digital converter to compensate for the output distortion."

Claim 10 of the first auxiliary request reads as follows:

"A compensating device for correcting output distortion of an analog to digital converter, comprising:  
a calibration device which, in a first state is arranged to receive a training signal and arranged to be adaptively configured to reduce a difference between a distortion signal and a simulated distortion signal;  
said calibration device, in a second state, being arranged to disconnect from an adaptation path and model distortion of the analog to digital converter using the configuration obtained during the first state;  
said calibration device, in said second state, being further arranged to generate an estimated distortion of the output of the analog to digital converter

a combiner configured to combine the output of the analog to digital converter with the estimated distortion of the output of the analog to digital converter, said estimated distortion fed forward from the calibration device, to compensate the output distortion."

Claims 2 to 9 are dependent on claim 1 and claim 11 is dependent on claim 10.

- IX. Claim 1, respectively claim 10, of the second auxiliary request adds the following feature to claim 1, respectively claim 10, of the first auxiliary request: "wherein the training signal is a noise signal that is random and uncorrelated."

Claims 2 to 9 are dependent on claim 1 and claim 11 is dependent on claim 10.

- X. Claim 1, respectively claim 10, of the third auxiliary request adds the following feature to claim 1, respectively claim 10, of the first auxiliary request: "wherein the output includes a plurality of output bits, the plurality of output bits include a plurality of higher order bits and at least one lower order bit that is separate from the plurality of higher order bits, and the estimation is based on a function of the plurality of higher order bits of the output."

Claims 2 to 9 are dependent on claim 1 and claim 11 is dependent on claim 10.

- XI. The appellant argued essentially as follows:  
In the invention, the calibration module was trained adaptively and the estimated distortion of the output

of the analog to digital converter (ADC) calculated by the calibration module was fed forward from the calibration module and combined with the output of the ADC to compensate for the output distortion of the ADC. D1 was focused on compensation of sensor distortions. It used a foreknowledge of the sensor nonlinear model but lacked knowledge of the model's parameter values. It was trained to acquire the numerical values of those parameters. D1 had nothing to do with linearizing ADCs. The system of D2 used feedback to correct nonlinearities. In the feedback path a digital signal was converted to an analog signal and subtracted from the input analog signal using a summing amplifier. The approach of the present application did not use feedback.

The block of the analog to digital converter shown in figure 7 of D3 eliminated coding redundancy inherent in each pipeline stage. It did not perform nonlinear cancellation or correction.

None of the documents D1, D2 and D3 disclosed, taught or even suggested an adaptive feedforward calibration module as defined in the claims of the present invention.

## **Reasons for the Decision**

1. The appeal is admissible.
2. *Inventive step (Article 56 EPC)*
  - 2.1 *Main request*
    - 2.1.1 The feedback path of D2 referred to by the appellant is the internal feedback path 239, 241b of the analog to digital multibit  $\Sigma$ - $\Delta$  modulator 216 (cf. figure 2). The



feedback signal is not used indeed to correct the nonlinearities (cf. D2, column 7, lines 35 to 46). Nevertheless D2 discloses an analog to digital converter ADC 236 wherein a corrected value  $\hat{y}_g(n)$  is fed forward and combined with the ADC output  $y(n)$  (cf. figure 2). During a training process, a dynamic error calibrator 280, called calibration module 280 in the following, adapts to compensate the error resulting from a comparison of the output  $y(n)$  of the analog to digital converter with a known input value 224. During steady state operation, the corrected value  $\hat{y}_g(n)$  is output by a nonlinear dynamic error estimator 250 and fed forward to be combined with the ADC output  $y(n)$ .

D2 is considered therefore as a relevant prior art.

2.1.2 D2 discloses in particular:

a method of correcting for output distortion of an analog to digital converter 236 (cf. D2, column 4, lines 6 to 26), comprising:

- receiving an output  $y(n)$  of the analog to digital converter at a calibration module 280 (cf. D2 figure 2; column 7, lines 25 to 34 and column 8, line 58 to column 9, line 22);
- training the calibration module 280 adaptively to estimate the output distortion and obtain an estimated distortion of an output of the analog to digital converter 236 (cf. D2, sections [0025] to [0027]), wherein:
  - the output  $y(n)$  includes a plurality of output bits (cf. D2, section [0021], column 7, line 27, and section [0023], line 47);
  - the plurality of output bits include a plurality of higher order bits and at least one lower order bit that is separate from the plurality of higher order bits (implicit);

the estimation is based at least in part on a function of the plurality of higher order bits of the output (implicit since the estimation is based on  $y(n)$  which comprises all output bits, cf. D2, section [0023]).

- 2.1.3 During the training process, the calibration module 280 of D2 receives the lag constants  $L_0, L_1, L_2...$  used by the nonlinear dynamic error estimator 251. On the basis of these constants, the calibration module calculates the coefficients that will be used subsequently by the estimator during the steady state operating mode to estimate the distortion  $\hat{y}_g(n)$  of the output of the ADC (cf. column 9, lines 16 to 30 and figure 2).

In steady state operating mode, the method according to D2 comprises the steps of:

- feeding forward the estimated distortion  $\hat{y}_g(n)$  of the output of the analog to digital converter 236 to a combiner 260 (cf. D2, figure 2); and
- combining the output  $y(n)$  of the analog to digital converter 236 with the estimated distortion  $\hat{y}_g(n)$  of the output of the analog to digital converter 236 to compensate for the output distortion (cf. figure 3e, step 344 and column 8, lines 21 to 30).

- 2.1.4 The nonlinear filter error estimator 251 of D2 comprises coefficients having both real and imaginary components or alternatively only real components (cf. D2, section [0028]), whereby the filter would become a linear filter.

Hence the subject-matter of claims 1 and 10 of the main request differs at most from the prior art disclosed in D2 in that "the nonlinear filter includes at least one linear filter coupled with at least one nonlinear element".

The subject-matter of claim 1 is therefore considered as new (Article 54 EPC).

2.1.5 The problem solved by this feature might be seen as providing an alternative to the nonlinear filter used in D2.

2.1.6 This novel feature is obvious having regard to D1 (cf. page 1, both columns and page 3, under "5. Discussion"). The nonlinear filter of D1 is composed only of linear filters and multipliers (cf. fig. 1 of D1) and D1 indicates that "distortions can be reduced ... by post processing of the sensor output signal ... using a general nonlinear filter structure to compensate the distortions of a whole class of nonlinear sensors" and that "this filter structure is not restricted to a special kind of sensor but can cover a whole class of nonlinear sensors. It is, in fact, a special case of the general Volterra filter with a significantly reduced complexity". Hence a person skilled in the art would have replaced the nonlinear filter of D2 by a general nonlinear filter according to D1 without exercising any inventive skill.

The invention as defined in claim 1 of the main request does not therefore involve an inventive step (Article 56 EPC).

## 2.2 *First auxiliary request (Article 56 EPC)*

2.2.1 Method claim 1 of the first auxiliary request specifies that the analog to digital converter is operated according to a first state and a second state and that an adaptation path in the calibration module is disconnected (during the second state operation). These features are known from D2 wherein the ADC is operated

according to a training state (calibration) and a steady state (cf. paragraph 2.1. above) and wherein the dynamic error calibrator 280 is disconnected during steady state operation (cf. D2, paragraph [0027]).

- 2.2.2 Finally the subject-matter of claim 1 of the first auxiliary request specifies that, during the second state, performing distortion correction includes "modeling distortion of the analog to digital converter using the configuration of the calibration module".

The calibration module 280 of D2 receives the same lag constants  $L_0, L_1, L_2, \dots$  as the lag constants used by the nonlinear filter error estimator 251 to calculate the coefficients to be stored in the look-up tables  $T_1, T_2 \dots$  of the nonlinear filter error estimator. At the end of each calculation of a set of coefficients, the calibration module 280 can be considered as configured. Its configuration i.e. the set of calculated coefficients is then transferred to the nonlinear filter error estimator (cf. D2, column 9, lines 22 to 30) which will model the distortion of the analog to digital converter during steady state operation. The configuration of the calibration module is therefore used to model the distortion of the analog to digital converter.

Furthermore despite the fact that the nonlinear filter error estimator 251 and the calibration module 280 are shown in figure 2 of D2 as two separate entities, a person skilled in the art would have also designed or represented the calibration module together with the nonlinear filter error estimator as one entity called calibration module without exercising any inventive step.

Thus the invention as defined by claim 1 of the first auxiliary request is not considered as involving an inventive having regard to D2 either (Article 56 EPC).

3. *Second auxiliary request (Article 56 EPC)*

Claim 1 of the second auxiliary request adds to claim 1 of the first auxiliary request that

"the training signal is a noise signal that is random and uncorrelated".

The calibration module i.e. the dynamic error calibrator 280 of D2 uses also a noisy signal in the form of an imperfect excitation signal which does not generate excessive noise (cf. D2, column 10, lines 40 to 53). Claim 1 of the second auxiliary request cannot therefore be seen as involving an inventive step over D2 either.

4. *Third auxiliary request (Article 56 EPC)*

Claim 1 of the third auxiliary request adds to claim 1 of the first auxiliary request that

"the output includes a plurality of output bits, the plurality of output bits include a plurality of higher order bits and at least one lower order bit that is separate from the plurality of higher order bits, and the estimation is based on a function of the plurality of higher order bits of the output."

- 4.1 The code issued by the code converter 217 of D2 comprises a plurality of bits (cf. figure 2 and section [0023], line 47) and a code comprising a plurality of bits comprises necessarily "a plurality of higher order bits and at least one lower order bit that is separate from the plurality of higher order bits".

4.2 Finally the remaining feature that "the estimation is based on a function of the plurality of higher order bits of the output" is known from D3 (cf. page 1866, right hand column, lines 5 to 9 and page 1871, first two paragraphs of section B in combination with figures 6 and 7) and a person skilled in the art would have applied the teaching of D3 and used only the higher order bits as input to the calibration module 280 of D2 to speed up the calibration process or to simplify the calibration module and filter error estimator of D2. The method according to claim 1 of the third auxiliary request is therefore considered as obvious in the light of the combination of prior art documents D2 and D3 (Article 56 EPC).

## Order

**For these reasons it is decided that:**

The appeal is dismissed.

The Registrar:

The Chairman:



U. Bultmann

M. Ruggiu

Decision electronically authenticated