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Datasheet for the decision of 17 October 2012

Case Number: T 0080/10 - 3.5.02

Application Number: 07000456.9

Publication Number: 1835623

IPC: H03L 7/081

Language of the proceedings: EN

Title of invention:
Delay locked loop circuit and semiconductor integrated circuit device

Applicant:
Renesas Electronics Corporation

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - auxiliary request (yes) - non-obvious alternative"

Decisions cited:
-

Catchword:
-

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Case Number: T 0080/10 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 17 October 2012

Appellant: (Applicant)
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 7 August 2009 refusing European patent application No. 07000456.9 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman: M. Ruggiu
Members: M. Léouffre
P. Mühlens

Summary of Facts and Submissions

I. The applicant lodged an appeal, received on 8 October 2009, against the decision of the examining division, posted on 7 August 2009, to refuse European patent application No. 07000456.9. The statement setting out the grounds of appeal was received on 17 December 2009.

II. The examining division held that claim 1 of the main request did not meet the requirements of Articles 123(2) and 54 EPC, and that claim 1 of the first and second auxiliary requests did not meet the requirements of Article 123(2) EPC.

III. The following documents of the state of the art have been cited during the procedure before the first instance:

D1: US 6 239 634 B1;

D2: US 2003/090296 A1;

D3: US 2004/264621 A1;

D4: US 6 867 627 B1; and

D5: David J Foley & al: "CMOS DLL-based 2-V 3.2-ps Jitter 1-Ghz Clock Synthesizer and Temperature-Compensated Tunable Oscillator", IEEE Journal of Solid-State Circuits, IEEE Service Center, Piscataway, NJ, US, Vol.36, no. 3, March 2001, XP011061463 ISSN: 0018-9200

IV. At the oral proceedings, which were held on 13 July 2009 before the department of first instance, the examining division made use of its discretionary power under Rule 137(3) EPC and did not admit the third auxiliary request. The reason for the decision was that, during the oral proceedings, the applicant disregarded

the invitation of the examining division to file only one further request and filed the third auxiliary request together with the second auxiliary request. The examining division held that this third auxiliary request did not prima facie address the objections raised under articles 83 and 84 EPC and communicated by phone on 23 June 2009.

V. With the grounds of appeal, received on 17 December 2009, the appellant filed the main and first auxiliary requests anew together with a second and a third auxiliary request based on the former third auxiliary request.

VI. In a communication, posted 20 July 2012 and accompanying a summons to oral proceedings, the board referred to document D6 = US 2005/0 231 249 A1 corresponding to the Japanese Patent Application Laid-open Publication no. 2005-311543 referred to as Patent Document 1 in the application as filed (cf. published application at section [0004]). The board gave its preliminary opinion that D6 deprived the independent claims of the main and first auxiliary requests of novelty and expressed the view that the second auxiliary request, based on the embodiment involving a one-shot pulse generator, could form a basis for a grantable patent.

VII. Oral proceedings before the board took place on 17 October 2012.

The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis

of claims 1 to 3 of the main request filed at the oral proceedings of 17 October 2012.
Furthermore, the appellant filed amended description pages 6a, 6b and 24 at the oral proceedings of 17 October 2012.

VIII. Claim 1 reads as follows:

"A delay locked loop circuit comprising:
a phase comparator (11);
a delay line (14) which changes a delay time given to a reference signal (Fr) on the basis of an output of the phase comparator and outputs a delayed reference signal as an output signal (Fo), and supplies the output signal as a feedback signal to the phase comparator, and
a control circuit (2) generating a control signal (s), wherein the phase comparator receives as inputs the reference signal, the feedback signal from the delay line and the control signal (s) which controls a start timing of a phase comparison operation between the reference signal (Fr) and the feedback signal (Fo) performed by the phase comparator,
wherein the delay locked loop circuit is adapted to inputting the reference signal (Fr) to the delay line (14) and to the phase comparator (11) at timings substantially equal to each other, and
wherein the control circuit (2) receives as input the reference signal (Fr) and outputs the control signal (s),
characterized in that
the control circuit (2) comprises a one-shot pulse generator (24) that generates a pulse and outputs the pulse as the control signal (s) when a first rising

edge of the reference signal is detected, and wherein an operation of the phase comparator (11) is reset by the one-shot pulse, and after said one-shot pulse, the control circuit (2) outputs a set signal as the control signal by which the phase comparator (11) is operated."

Claims 2 and 3 depend on claim 1.

IX. The appellant essentially argued as follows:

The subject-matter of claim 1 was based on the pulse generator embodiment shown in figures 4 and 6 and original claim 4. The substance of this original claim was never objected. It was addressed only by the summarizing statement in item 2.4 of the extended European Search Report of 13 June 2007: "the remaining claims only seem to contain design features, which come within the scope of customary practice followed by persons skilled in the art, Articles 52(1) and 56 EPC". Similarly, item 3. of 24 February 2009, quoting earlier items 2 to 2.4 raised no substantiated objection.

Reasons for the Decision

1. The appeal is admissible.

2. *Admissibility of the request*

The appellant requests the grant of a patent on the basis of the second auxiliary request filed with the grounds of appeal.

This second auxiliary request corresponds to the non-admitted third auxiliary request filed at the oral proceedings before the department of first instance. The examining division exercising its discretionary power under Rule 137(3) EPC referred to objections raised in a telephone conversation of 23 June 2009.

The Board notes however, that following the amendments to the claims (third auxiliary request filed on 13 July 2009) and to the description received on 2 July 2009, the Articles 83 and 84 EPC objections did not apply. The third auxiliary request concerned a particular embodiment of the invention and was based on original claim 4, which was searched and was never objected as to its substance. The third request should have therefore been seen as a valid attempt to overcome the objections of lack of novelty raised against the previous requests.

The present request is therefore admitted into the procedure.

3. *Amendments*

3.1 The feature objected by the examining division: "the delay locked loop circuit is adapted to adjust a timing at which the reference signal (Fr) is inputted to the delay line (14) and a timing at which the reference signal (Fr) is inputted to the phase comparator (11) such that they are substantially equal to each other" has been reworded to: "wherein the delay locked loop circuit is adapted to inputting the reference signal (Fr) to the delay line (14) and to the phase comparator (11) at timings substantially equal to each other".

This feature is similar to the feature of original claim 1: "wherein a timing at which the reference signal is inputted to the delay line and a timing at which the reference signal is inputted to the phase comparator are substantially equal to each other". The remaining features of claim 1 are based on original claims 1, 2 and 4 whereby the "pulse generator" is specified as a "one-shot pulse generator". A basis therefor can be found in section [0053].

The description of the application has been amended to be consistent with the claims and to acknowledge the background art disclosed in documents D1 and D3.

Thus, the amendments to the application do not contravene Article 123(2) EPC.

4. *Novelty*

Document D6 is considered as representing the closest prior art. It discloses:
a delay locked loop circuit 20 comprising (cf. figures 2 to 4 and the title of D6):
a phase comparator 101;
a delay line 104 which changes a delay time given to a reference signal CLK on the basis of an output of the phase comparator 101 and outputs a delayed reference signal as an output signal, and supplies the output signal as a feedback signal to the phase comparator (cf. sections [0038] and [0039]).

D6 discloses in figure 4 a control circuit 205, comprising a counter and a two-input AND gate 307, controlling a start timing of a phase comparison

operation between the reference signal CLK and the feedback signal performed by the phase comparator.

The representations of the control circuit 205 and the phase detector 101 of D6 differ from the representations of the control circuit and the phase detector of the present application because in D6 the AND-gate 307 is represented as belonging to the control circuit 205. However the AND-gate can be regarded as belonging to the phase detector and the control circuit as comprising only the counter 206 generating the control signal. The phase comparator comprises then the elements 101 and 307 and receives as inputs the reference signal CLK, the feedback signal from the delay line and the control signal (output of counter 306) like in the present application.

The reference signal clock is applied to the delay line and to an input of the AND-gate 307 of D6 at timings substantially equal to each other.

The counter 306 of D6 receives as input the reference signal CLK and counts edges of the reference signal. It outputs a set signal as the control signal by which the phase comparator is not operated until the count number of the counter reaches a set value, and outputs a set signal as the control signal by which the phase comparator is operated after the count number of the counter reaches the set value (cf. "predetermined number" in section [0048]).

The subject-matter of claim 1 differs from D6 in that "the control circuit (2) comprises a one-shot pulse generator (24) that generates a pulse and outputs the

pulse as the control signal (s) when a first rising edge of the reference signal is detected, and wherein an operation of the phase comparator (11) is reset by the one-shot pulse, and after said one-shot pulse, the control circuit (2) outputs a set signal as the control signal by which the phase comparator (11) is operated".

Among the other documents cited in the procedure D3 is the only document providing a pulse control signal (RSTb) (cf. figure 3 and sections [0014] and [0015]). In D3, the pulses are generated at each comparison of the phases of the reference signal and the delayed feedback signal. The pulse control signal of D3 is thus a repeating pulse signal and not a one-shot pulse signal.

The subject-matter of claim 1 is therefore new when compared to the available prior art (Article 54 EPC).

5. *Inventive step*

A one-shot pulse generator is not disclosed in any of the documents cited in the procedure. A combination of the available documents, as e.g. D3 and D1, would therefore not lead to the characterising part of claim 1.

The subject-matter of claim 1 is also not obvious when starting from the closest prior art represented by D6. D6 discloses a delay locked loop circuit which could be represented by a block diagram similar to the block diagram shown in figure 15 of the present application. The block diagram of figure 15 is detailed in figure 18 which shows the control signal (s) applied to a NAND

gate 111 receiving the reference signal (Fr) as a second input. The phase frequency comparator of figure 18 is enabled when the control signal (s) is at a high level and remains at a high level (cf. section [0039] of the published application). The simple replacement of the step signal s of figure 18 with a pulse signal followed by a step signal is unlikely to lead to an operable delay line circuit.

In the same way, replacing the control signal of D6 with a one-shot pulse signal followed by a step signal and applying the newly created control signal to an input of AND-gate 307, which receives the reference signal (Fr) as a second input, would not lead to an operable delay line circuit.

Actually the one-shot pulse generator is used in combination with the circuit shown in figure 19 which replaces the circuit of figure 18, and neither the amendments to the circuit of figure 18 necessary to arrive at the circuit of figure 19 nor the circuit generating a one-shot pulse signal to reset the phase comparator, followed by a set signal enabling the phase comparator (cf. figures 6 and 25) appear to be obvious.

There is no incentive for a person of ordinary skill to develop a circuit as disclosed in figures 6 and 19 of the present application or to modify the circuit of D6 accordingly. Hence, in the light of the available prior art, in particular D6, the solution proposed in the present application is not obvious in the sense of Article 56 EPC.

6. The subject-matter of claims 2 and 3, which are dependent on claim 1 is also to be considered as being new and involving an inventive step.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

claims: 1 to 3 of the main request filed at the oral proceedings of 17 October 2012,

description: pages 1 to 6, 7 to 23, and 25 to 30 filed with letter of 17 September 2012; pages 6a, 6b and 24 filed at the oral proceedings of 17 October 2012,

drawings: sheets 1/16 to 16/16 as originally filed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu