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Datasheet for the decision of 27 September 2013

Case Number: T 2447/09 - 3.5.06

Application Number: 98112385.4

Publication Number: 889393

IPC: G06F 9/34, G06F 9/30

Language of the proceedings: EN

Title of invention:
Force page zero paging scheme for microcontrollers

Applicant:
Microchip Technology Incorporated

Headword:
Force page zero access/MICROCHIP

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step - after amendment (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 2447/09 - 3.5.06

D E C I S I O N
of the Technical Board of Appeal 3.5.06
of 27 September 2013

Appellant: (Applicant)
Microchip Technology Incorporated
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 22 June 2009 refusing European patent application No. 98112385.4 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: D. H. Rees
Members: M. Müller
C. Heath

Summary of Facts and Submissions

I. The appeal lies against the decision of the examining division, with written reasons dispatched on 22 June 2009, to refuse the European patent application no. 98 112 385.4 for lack of clarity, Article 84 EPC 1973, and lack of an inventive step, Article 56 EPC 1973, over the document

D1: Stevens K. W., "Addressing a Second Page of Registers without Increasing the Register Field Length", IBM Technical Disclosure Bulletin, Vol. 16, No. 3, August 1973,

and, as regards the auxiliary request, for lack of conformance with Article 123 (2) EPC.

II. A notice of appeal was filed on 17 August 2009, the appeal fee being paid on the same day. A statement of grounds of appeals was received on 20 October 2009. The appellant requested that the decision under appeal be set aside and that a patent be granted based on claims 1-14 or 1-12 according to a main or auxiliary request, respectively, as filed with the grounds of appeal.

III. With a summons to oral proceedings, the board informed the appellant about its preliminary opinion according to which the claims lacked clarity and an inventive step over D1, Article 56 EPC 1973.

IV. In response to the summons, with letter of 27 August 2013, the appellant submitted amended claims according to a main and two auxiliary requests, and a new docu-

ment so as to establish the fact that the term "special function registers" was a term of the art:

E1: "Microcomputer Components, Microcontrollers, Data-Catalog 1990", excerpt related to the "8-Bit Single Chip Microcontroller SAB 80515/80535", pages 108-117, Siemens, 1990.

V. Oral proceedings were held as scheduled on 27 September 2013, during which the appellant filed a further document, which the board refers to as E2, to illustrate its view on the differences between D1 and the microcontroller architecture on which the invention is based:

E2: Tietze U et al., "Halbleiter-Schaltungstechnik", Springer-Verlag, pages 596-597 and 630-634, 1986

The appellant also filed further amended claims 1-14 as a new main request. The previous main request was dropped, whereas the previous second auxiliary request was maintained as the new sole auxiliary request. The appellant requested the grant of a patent based on the following application documents:

claims, no.
1-14 according to the main request as filed during oral proceedings on 27 September 2013, or
1-15 according to the auxiliary request, filed as "2nd auxiliary request" on 27 August 2013
description, pages
1-5 as filed on 24 October 2008
drawings, sheet
1 as originally filed

VI. Independent claims 1 and 8 of the main request read as follows:

"1. A method of accessing a data memory page in a data random access memory for a microcontroller comprising a linearized data random access memory which is divided into a plurality of data memory pages, the method comprising the steps of:

mapping special function registers only to a single predefined page (24) of said data memory pages;

selecting one of said data memory pages by means of a page select register to provide data random access memory for said microcontroller;

dedicating a bit (36) in each op-code of at least numeric processing instructions (30) of said microcontroller which when set forces said predefined page (24) to be selected as data random access memory (22) storing said special function registers and when not set accesses said selected one of said data memory page."

"8. A microcontroller having a memory page architecture comprising, in combination:

data random access memory (22) having an entire linearized address range wherein said data random access memory (22) is divided into a plurality of memory pages, wherein special function registers are memory-mapped only to a single predefined memory page;

a page select register for selecting a current memory page; and

a dedicated bit (36) in each opcode of at least numeric processing instructions (30) of said microcontroller which when set forces said predefined memory page (24) to be selected instead of said

currently selected memory page as data random access memory (22) storing said special function registers and when not set accesses the currently selected memory page."

VII. At the end of the oral proceedings, the chairman announced the board's decision.

Reasons for the Decision

The invention

1. The application relates to microcontrollers using a random access memory (RAM) paging scheme, in particular to those of the PIC family (see original description, page 1, line 15).

1.1 Paging is an established method of memory management according to which the memory is divided into so-called "pages" and a memory location is addressed by selection of the pertinent page and an offset within that page. The addresses in the microcontroller instructions are limited to the bits representing the offset and a dedicated register is provided for selecting the page relative to which the offset is interpreted. This register is called the "page select register" (see page 2, lines 13-14 and page 3, line 4). Pages are also known as "banks" (see page 2, lines 1-5; page 5, lines 5-13 and fig. 1). For instance, the PIC microcontrollers use the term "bank" instead of "page" and "bank select register" instead of "page select register".

1.2 Microprocessors and microcontrollers are known to contain special registers which control or monitor the microprocessor's function, for example relating to IO or peripheral control or to the processor status. In the description, these registers are referred to as "special function registers" (SFR), the term used, *inter alia*, in the microcontrollers of the PIC family and in E1 (see *e.g.* page 115, section "Data Memory"). According to the PIC microcontroller architecture the SFRs are held in RAM.

1.3 It is important that the SFRs can be accessed quickly, for example during an interrupt service routine. For this reason it was known, according to the application (page 2, lines 1-4), to replicate the SFRs in every page of RAM so that access to the SFRs was possible at all times within the currently selected page. This however constituted a waste of precious memory space (page 2, line 4-7).

1.4 As a solution to this problem, the application describes the provision of a "dedicated bit in each op-code instruction of the microcontroller" which bypasses the page select register and "forces access" to a predefined page (typically the first one, page zero; see page 4, lines 7-11). The special function registers are all mapped to this page so that it becomes possible to access them quickly "at all times" without replicating them in all pages. The claims do not require this dedicated bit for "each op-code" but only for the "numeric processing instructions".

Article 123 (2) EPC

2. In the decision under appeal, an objection against then independent claims 1 and 7 of the auxiliary request was made (see reasons 17) due to a feature which was also contained in claims 7 and 14 of the then main request. In response to the board's preliminary opinion the appellant discarded the pertinent features from the claims. This objection has thus become moot.

3. Amended claims 1 and 8 of the main request are based on original claims 1 and 11. The additional feature that "at least numeric processing instructions" shall have the dedicated bit is disclosed on originally filed page 7 (lines 21-23). The original application does not explicitly state that the SFRs are mapped "only" to a single predefined page. The description does disclose that, according to the invention, "[t]he first page ... is used for storing the SFRs" (page 6, lines 5-7) and that, via the "dedicated bit", the "current instruction will always affect the first page ... which stores the special and general purpose registers" (page 6, line 24 - page 7, line 2). The description qualifies the latter statement by the phrase "no matter where the user is in the RAM" and refers to the microcontroller "go[ing] back to the current address" (loc. cit. and page 7, lines 8-11), thereby suggesting that the first page is different from the rest of the RAM. In the board's judgment, the skilled person will understand the description as a whole to imply, directly and unambiguously, that the invention maps the SFRs "only" to the first - *i.e.* the single predefined - page. In view of this, the board is satisfied that the claims of the main request conform with Article 123 (2) EPC. Whether

this also holds for the claims of the auxiliary request is irrelevant in view of the outcome of this appeal.

Article 84 EPC 1973

4. In the decision under appeal, the then claims were found unclear for three reasons.

4.1 The reference to data memory pages to be "select[ed] ... to provide data random access memory" did "not make sense" since "memory cannot be provided" but "it is rather the memory which provides data" (reasons 14.01). The board does not share this concern. The page select register selects one page of memory as the context in which the offset bits in the instructions are to be interpreted. The skilled person would understand that in this sense the selected page is "provided [as] data random access memory for the microcontroller".

4.2 The reference to a page "to be selected as data random access memory" was unclear because it suggested that a page could also be selected in another way which was however not disclosed (reasons 14.02). The board does not share this concern either. As explained, the invention relates to the selection of a memory page as the relevant context for the interpretation of the offsets in microcontroller instructions. When set, the dedicated bit determines the selection of a "predefined page" which makes it, as the skilled person would understand, the present "data random access memory". The skilled person would understand that it is in this sense that the page is "selected *as* data random access memory".

4.3 The claim wording left unclear "which is the actual instruction executed by the microcontroller" (reasons 14.03). Present claims 1 and 8 as amended refer to "instructions" only once. The second reference to "instruction being executed by said microcontroller" was discarded and a reference to the "page select register" was inserted instead. The board deems the amended wording to be clear.

4.4 The board therefore comes to the conclusion that independent claims 1 and 8 are clear, Article 84 EPC 1973, and also has no clarity objections against dependent claims 1-7 and 9-14.

The documented prior art

5. D1 was the only prior art document cited during examination.

5.1 D1 relates to the instructions of a microprocessor operating on one or two registers within a page of registers. Normally 4 bits are available to address each register, but in some situations the instruction word contains additional spare bits (see esp. the register-to-register half word instruction explained on page 772, 2nd par., lines 3-6). These bits are used to address additional pages of registers and are hence referred to as "page bits" and marked as "P" in the figure. More specifically, the page bits are used to select one of two page pointer registers (a "default" one or a "second" one, see page 772, first full par., last three lines) the contents of which, in turn, identify one of two pages of operand registers (see sentence bridging

pages 771-772 and page 772, first full par., lines 6-15: "default page" and "second page").

5.2 D1 makes a distinction between registers and memory (see *e.g.* the register-to-memory instruction), thereby suggesting that register are not held in RAM.

Article 56 EPC 1973

6. In the decision under appeal the assessment of inventive step starts from (and is exclusively based on) D1. *Inter alia*, it is observed (at 15.02) that D1 does not mention special and general purpose registers to be stored "in one of the two pages" of registers according to D1 but it "the use of the registers of each page is" argued to be "a mere design choice" which would "produc[e] no further technical effect".

6.1 The board agrees that the addressing scheme according to D1 is unaffected by what is actually stored in the pages. The board disagrees however that the reference to the special function registers in the independent claims can be dismissed as producing no "further" technical effect.

6.2 The board agrees with the appellant that the term "special function registers", even if broad, has an established meaning in the art of microprocessors (and microcontrollers) implying their importance for the functioning of the microprocessor, *e.g.* as regards IO routines or interrupt service routines. In this context, the ease and speed of access available to special function registers is relevant and therefore, in the board's judgment, does produce a technical effect which

must be taken into account in the assessment of inventive step.

6.3 D1 neither mentions SFRs explicitly nor, to the extent that they might be considered implicit in the microprocessor to which D1 relates, where the SFRs are stored. D1 alone therefore would not, in the board's judgment, have prompted the skilled person to "[map] special function registers only to a single predefined page" (*e.g.* to page zero) and to have one of the two "page pointer registers" point to that page (*e.g.* by storing the constant "0" in the "second page point register).

6.4 The board therefore comes to the conclusion that the claimed invention is not obvious over D1 alone.

7. Given the central importance of the SFRs for the invention, the board considers that a more appropriate starting point for the assessment of inventive step is the microcontroller discussed in the application which maps the special function registers in every page (page 2, lines 1-5, and page 5, lines 5-13). For convenience, this microcontroller is referred in the following as "the PIC microcontroller".

7.1 The claimed invention differs from the PIC microcontroller in the following three respects:

a) The SFRs are not replicated but mapped to a single predefined memory page;
b) some instructions provide a "dedicated bit" which when set forces access to another page than that defined in the page select register; and

c) that other page is the one to which the SFRs are mapped.

7.2 Feature a) solves the problem of avoiding the "waste of precious RAM space", as the application puts it.

7.3 Feature b) solves the problem of extending the address space that can be conveniently addressed beyond the single page defined by the page select register.

7.4 Feature c) links features a) and b) in that the dedicated bit according to feature b) is used in order to provide a convenient access to the single predefined memory page according to feature a). Feature c) establishes that features a)-c) in combination solve a joint technical problem.

In the board's view, this technical problem - solved by the claimed invention as a whole over the PIC microcontroller - can be seen as how to maintain easy access to the SFRs while reducing their space requirements.

Re. difference a)

8. That the replication of SFRs wastes RAM space would, in the board's view, be obvious for the skilled person and so would be the solution to confine the SFRs to only a single predefined page. Access to the SFRs would remain possible "at all times" without further ado, although much less convenient: If an instruction were to access an SFR in the context of a routine operating on a selected memory page, it would have to save the contents of the page select register, override it with the number of the predefined page, access the SFR in question,

then retrieve the stored page number and restore it to the page select register before continuing with the main routine. While the board tends to agree with the appellant that this solution might be unattractive and therefore not be produced for the market, it disagrees with the appellant's allegation that this would make the solution any less obvious from a technical perspective. The board therefore considers that mapping SFRs "only to a single predefined memory page" would be obvious for the skilled person according to the described trade-off between memory requirements and convenience of access.

Re. difference b)

9. D1 is, as exemplified by its title, primarily concerned with addressing more register pages within the limits of a given register field length.

9.1 The appellant stresses that D1 relates to registers as opposed to data memory and therefore does not disclose a paging scheme for pages of data memory. This difference is, according to the appellant, an indication of the fact that D1 relates to a different microprocessor architecture than the invention: In the architecture according to D1, the microprocessor provided a large number of registers on-chip whereas the simpler PIC architecture provided only a single "working register" on chip (also known as an "accumulator") and held the special purpose registers in RAM. E2 was introduced for illustration of this issue.

9.2 The board has no reason to doubt the appellant's interpretation of D1 and therefore accepts that D1 discloses

an addressing scheme for pages of registers as opposed to the invention which relates to an addressing scheme for pages of RAM. It is thus not necessary to make detailed reference to E2.

9.3 Nonetheless, the board disagrees that this difference alone would disqualify D1 as a teaching that the skilled person would refer to when starting from the PIC microcontroller.

9.4 D1 does not only teach to enlarge the number of addressable register pages by the introduction of the page bits. Rather, the two page pointer registers also enable quick access to two selected register pages at the same time rather than just one, and the skilled person would realize that this effect existed also if the two register pages were selected from the same register address space.

9.5 If the skilled person, starting from the PIC microcontroller with RAM paging, were interested in convenient access to two pages of memory rather than only one, he would, in the board's view, not hesitate to adapt the addressing scheme according to D1 for integration into the microcontroller by providing a second page select register and page bits in at least some of the microcontroller instructions to chose between the page select registers.

10. The board therefore considers that the two modifications of the PIC microcontroller discussed above would both be obvious for the skilled person but for separate reasons: Limiting the SFRs to a single, predefined page would be obvious in order to save RAM space (see point

7.2 above) and the incorporation of the addressing scheme of D1 would be obvious in order to provide convenient access to two RAM pages at the same time (see point 7.3 above). The PIC microcontroller so modified (henceforth "the modified PIC microcontroller") would have features a) and b) but still not fall within the scope of the independent claims due to lack of feature c): The page bits would not provide forced access to the predefined page holding the SFRs. The modified PIC controller would therefore not solve the technical problem formulated in point 7.4 above.

Re. difference c)

11. As already suggested, this forced access *could* be implemented in the modified PIC microcontroller: If the predefined page were page zero it would suffice to store the value "0" constantly in the second page select register to achieve the claimed force page zero effect according to the invention. It follows that the skilled person starting from the PIC microcontroller *could* have arrived at the claimed invention in view of D1. It would also appear arguable that the claimed invention lacks an inventive step over the *modified* PIC microcontroller.

11.1 This is, however, not the question to be assessed in the present case. It must be decided whether it *would* have been obvious for the skilled person to arrive at the claimed invention starting from the *unmodified* PIC microcontroller, *i.e.* with RAM paging, a single page select register and replicated SFRs.

11.2 The board considers that, starting from the unmodified PIC microcontroller, the skilled person would not have had sufficient reason to resort to D1 in order to solve the above-mentioned problem. More specifically, it would not have been obvious for the skilled person to refer to the teaching of D1, modify and incorporate it into the PCT microcontroller in order to alleviate the trade-off between the space needed to store the SFRs and the time needed to access them and thus to make the one page solution more attractive.

11.3 Hence, even though the skilled person could have arrived at the claimed invention starting from the PIC microcontroller in view of D1 it would not have been obvious for him to do it without exercising an inventive step. The board thus concludes that the subject matter of claims 1 and 8 according to the main request show the required inventive step, Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent as follows:

   - Claims 1-14 of the main request as filed during oral proceedings;
   - description pages 1-5 filed on 24 October 2008;
   - drawing sheet 1 as originally filed.

The Registrar: The Chairman:

B. Atienza Vivancos D. H. Rees