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Datasheet for the decision of 18 June 2013

Case Number: T 2366/09 - 3.4.03

Application Number: 98945781.7

Publication Number: 963604

IPC: H01L 21/768, H01L 21/321

Language of the proceedings: EN

Title of invention:
High density plasma oxide gap filled patterned metal layers with improved electromigration resistance

Applicant:
ADVANCED MICRO DEVICES, INC.

Headword:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56, 84

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 2366/09 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 18 June 2013

Appellant: (Applicant)
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 28 July 2009 refusing European patent application No. 98945781.7 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
T. Bokor

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 98 945 781 for lack of clarity, Article 84 EPC.

II. Summons to oral proceedings before the board, requested by the appellant applicant, were issued on 22 January 2013 with an annex containing objections including lack of clarity, added subject-matter and lack of an inventive step against claims 1 to 23 filed with the statement setting out the grounds of appeal.

In a letter dated 13 May 2013, in reply to these summons, the appellant stated "*We [...] file herewith claims 1- 25 [sic] to replace claims 1 - 25 [sic] filed with the Grounds of Appeal, and arguments in support of the newly filed claims*".

In fact, new claims 1 to 23 were annexed to this letter, replacing claims 1 to 23 filed with the statement setting out the grounds of appeal.

The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims filed with the letter of 13 May 2013.

Moreover, in a further letter dated 12 June 2013, the board was informed that the applicant would not be represented at the oral proceedings.

Oral proceedings before the board took place on 18 June 2103 in the absence of the appellant.

III. Claim 1 reads as follows:

"*A method of manufacturing a multi-level semiconductor device, which method comprises:*
forming a first dielectric layer on a semiconductor substrate;
forming a first metal layer on the dielectric layer, wherein the first metal layer is patterned to form gaps between metal features;
depositing a high density plasma oxide in said gaps by high density plasma chemical vapour deposition;
performing a first heat treatment in an inert atmosphere at a first temperature of about 350°C to about 450° C for a first period of time of about 45 minutes to about 2 hours, to substantially increase the grain size of the first patterned metal layer, thereby increasing the electromigration resistance of the first patterned metal layer; and
performing a second heat treatment in an atmosphere comprising nitrogen and hydrogen in an amount of about 5% to about 15 volume % of hydrogen at a second temperature of about 300°C to about 400°C for a second period of time of about 30 minutes to about 1 hour, wherein the second heat treatment is performed at a second temperature lower than the first temperature for a second period of time shorter than the first period of time."

IV. Reference is made to the following documents:

D1: S. Bothra et al: "*Integration of 0.25um three and five level interconnect system for high performance ASIC*", Proceedings of VMIC Conference, 1997 ISMIC, 10-12 June 1997, pages 43-48

D2: US 5 300 307 A

D3: US 4 352 239 A.

V. The appellant submitted in substance the following arguments:

The specification was not inconsistent with regard to the effect of the different heat treatments, but reflected the inventors' experimental results. Irrespective of the overlap in time and temperature between the heat treatments, the difference in atmosphere might very well account for the different results, particularly since the hydrogen had a penetrating effect.

Moreover, there was no teaching in D1, D2 or D3 to suggest the fact that the conventional densification heat treatment of an SOG gap filling layer in fact caused grain size growth. In fact, this would not be expected by the teachings of D2 and D3 which used heat treatment of the exposed metal and in a forming gas atmosphere to produce such a result. It was applicants' recognition of that fact, which led applicants to the claimed first heat treatment step in an inert atmosphere, which was similar to the densification heat treatment for a SOG gap filled article. Accordingly, the subject-matter of claim 1 involved an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Procedural issues*

The amended new claims 1 to 23 were filed after oral proceedings before the board were arranged.

In view of the fact that the amendments were filed in advance of the oral proceedings, constitute an attempt to overcome the objections raised and are provided with reasons in support thereof, and as the board is satisfied that it is able to deal with the request in substance, without adjournment of the oral proceedings, the new request is admitted into the proceedings (Article 13(1) and (3) RPBA).

3. *Amendments*

Claim 1 is based on claims 1, 2 and 5 as originally filed.

Accordingly, the amendments to claim 1 comply with Article 123(2) EPC.

In particular, it is noted that claim 1 as amended contains the feature "*wherein the second heat treatment is performed at a second temperature lower than the first temperature for a second period of time shorter than the first period of time*". This feature stems from claim 1 as originally filed and overcomes the objection of added subject-matter raised in the annex to the summons to oral proceedings.

4. *Clarity*

As noted in the annex to the summons to oral proceedings, in the decision under appeal lack of clarity, Article 84 EPC (or even insufficiency of disclosure, Article 83 EPC) was argued under points 1.4 to 1.6, noting that according to the description a conventional annealing at a temperature of about 350 °C to about 400 °C for a period of time up to about one hour in an atmosphere of nitrogen and hydrogen in amounts of about 10% by volume was insufficient to cause any significant grain growth of patterned metal layers (page 6, lines 12 to 19). Yet according to claim 1, the method comprised performing a first heat treatment in an inert atmosphere at a first temperature of about 350 °C to about 450 °C for a first period of time of about 45 minutes to about 2 hours, to substantially increase the grain size of the first patterned metal layer.

The appellant argued in this respect that the specification was not inconsistent, but reflected the inventors' experimental results. Irrespective of the overlap in time and temperature, the difference in atmosphere might very well account for the different results, particularly since the hydrogen had a penetrating effect.

It is, however, noted that the above suggestion of the appellant on the possible impact of hydrogen is not supported by the application, which is silent on any effect of the atmosphere during the heat treatment.

Rather, it would appear from the application that it is the fact that the heat treatment is more severe in terms of temperature and time than the conventional annealing step that causes an increase in grain size, with an attendant improvement in electromigration resistance (page 6, line 12 to page 7, line 4).

In fact, as pointed out in the decision under appeal, according to eg document D2, an increase in grain size in aluminium is obtained with a heat treatment at 425 °C for 35 minutes in an atmosphere containing hydrogen (column 4, lines 13 to 19).

Yet it may be accepted in the present case for the purposes of this decision that since the skilled person knows that an increase in grain size causes an increase in electromigration resistance, and both increases are easily verified, based on the definitions in claim 1 of the results to be achieved by the first heat treatment "*to substantially increase the grain size of the first patterned metal layer" and "thereby increasing the electromigration resistance of the first patterned metal layer*", it would be sufficiently clear to the skilled person which temperatures and times within the specified ranges of claim 1 are intended.

Similarly, it may be accepted that it would be sufficiently clear to the skilled person which temperatures and times for the second heat treatment within the specified ranges of claim 1 are intended.

5. *Novelty*

Document D1 discloses a method of manufacturing a multi-level semiconductor device comprising, in the wording of claim 1,
forming a first dielectric layer (HDP, PECVD) on a semiconductor substrate;
forming a first metal layer (M1) on the dielectric layer, wherein the first metal layer is patterned to form gaps between metal features;
depositing a high density plasma oxide (HDP) in said gaps by high density plasma chemical vapour deposition (cf page 44, lines 17 to 43; table 1; figure 1).

The subject-matter of claim 1 differs from D1 in that the following two heat treatment steps are specified:

- performing a first heat treatment in an inert atmosphere at a first temperature of about 350 °C to about 450 °C for a first period of time of about 45 minutes to about 2 hours, to substantially increase the grain size of the first patterned metal layer, thereby increasing the electromigration resistance of the first patterned metal layer; and

- performing a second heat treatment in an atmosphere comprising nitrogen and hydrogen in an amount of about 5% to about 15 volume % of hydrogen at a second temperature of about 300°C to about 400°C for a second period of time of about 30 minutes to about 1 hour, wherein the second heat treatment is performed at a second temperature lower than the first temperature for a

second period of time shorter than the first period of time.

Accordingly, the subject-matter of claim 1 is new over document D1 (Article 54(1) EPC 1973). The subject-matter of claim 1 is also new over the remaining, more remote prior art.

6. *Inventive step*

6.1 As noted in the annex to the summons to oral proceedings, regarding the first heat treatment, according to the application, the reason for conducting this heat treatment is that "*Upon experimentation and investigation, it was found that the conventional "annealing" step was insufficient to cause any significant grain growth of patterned metal layers. Since HDP-CVD does not require a relatively severe heat treatment for densification, as does SOG, and the conventional "annealing" step is insufficient to increase the grain size of the patterned metal layers, it was concluded that a patterned metal layer gap filled with SOG exhibits greater electromigration resistance than a patterned metal layer gap filled with a HDP oxide, because of the relatively severe densification baking performed after SOG deposition which induces grain growth of the gap filled patterned metal layer*" (cf page 6, lines 17 to 24). Accordingly, "*a heat treatment step is performed under conditions paralleling a conventional SOG baking treatment of about 350 °C to about 450 °C for about 45 minutes to about 2 hours, to substantially increase the grain size of the gap filled patterned metal layers for improved*

electromigration resistance" (cf page 6, lines 26 to 29).

The second heat treatment step is a conventional annealing in a forming gas atmosphere which, as also indicated in the application, is typically conducted after formation of all patterned metal layers to remove radiation damage, drive out moisture and neutralize trapped charges (cf description, page 6, lines 12 to 17).

The above distinguishing features are considered to independently solve two respective partial problems.

Accordingly, having regard to the first heat treatment, the objective partial problem to be solved relative to D1 is to improve electromigration resistance.

Having regard to the second heat treatment, the objective partial problem to be solved relative to D1 is to remove radiation damage, drive out moisture and neutralize trapped charges.

6.2 Regarding the above first partial problem, it is noted that a person skilled in the art, working in the field of multilevel metallization for VLSI devices, would be familiar with the problems of electromigration and in particular with the fact that grain growth in the metal layer is necessary to reduce electromigration and that grain growth is achieved by a heat treatment. Reference is made in this respect to for instance document D3 (see in particular column 1, lines 33 to 39; column 1, line 55 to column 2, line 44; column 3, line 10 to column 4, line 7). It is, moreover, noted that D1

specifically reminds of the problem of electromigration (cf page 45, first paragraph).

Accordingly, it would be obvious to the skilled person to provide a heat treatment as claimed to achieve grain growth in the method of D1, thereby improving electromigration resistance. It is noted in this respect that a suitable temperature and duration for such a heat treatment would be arrived at by straightforward experimentation falling within the competence of the skilled person.

6.3 The appellant argued that D3 as well as D2 both taught methods of increasing grain size growth by heat-treating a patterned metal layer after it had been created, but before it was covered with other layers. Dl did refer to the problem of electro migration, but did not teach anything about grain size growth to address the issue. Dl expressed a need to configure the physical layout of the stack/metal component structure to minimize electro migration. There was no teaching in Dl, D2 or D3 to suggest the fact that the conventional densification heat treatment of an SOG gap filling layer in fact caused grain size growth. In fact, this would not be expected by the teachings of D2 and D3 which used heat treatment of the exposed metal and in a forming gas atmosphere to produce such a result. Applicants discovered the unexpected fact that the densification heat treatment of SOG in fact caused grain size growth. It was applicants' recognition of that fact, which led applicants to the claimed first heat treatment step in an inert atmosphere, which was similar to the densification heat treatment for a SOG gap filled article. Such a step was not employed in

connection with prior art HDP oxide CVD gap filling, because the SOG type densification was not required and the side effect on grain size of such densification was not recognized.

These arguments, however, are not found convincing. Although it is true that eg document D3 concerns a metal layer, which is not (yet) covered by a dielectric layer, there is nothing suggesting that the teaching of D3 on grain growth would be affected by the presence of a covering dielectric layer. Accordingly, it would be obvious to the person skilled in the art to attempt applying the teaching of D3 to the method of D1 in order to deal with electromigration, flagged in D1 to be a problem to be addressed. The fact that D1 mentions that the metal stack is optimized to provide a high electromigration resistance is not regarded as keeping the skilled person from considering other solutions for increasing electromigration resistance suggested in the prior art. The remaining arguments of the appellant are based on a method using spin-on-glass (SOG) followed by a baking treatment as the starting point of the invention. The board's assessment, however, starts from the closer prior art provided by document D1 in which HDP CVD oxide is already used, so that these arguments are beside the point. Still even if the skilled person were to consider a method using SOG, the fact that the densification heat treatment of SOG causes grain size growth cannot reasonably be held to be unexpected to the skilled person. As noted above, it is well known to the skilled person that heat treatments cause grain growth in the metal layer and thereby an increase in electromigration resistance. Moreover, it is also commonly known that all heat treatments to which the

metal layer is subjected in the course of the manufacturing process up to completion of the device are to be taken into account. If the SOG baking step is eliminated because of the use of another material, it would readily occur to the skilled person, and moreover be easily verifiable, that this will have an impact on grain growth and that, if needed, a heat treatment should be introduced to compensate for it.

6.4 Regarding the above second partial problem, since, as noted above, the second heat treatment step is a conventional annealing in a forming gas atmosphere for removing radiation damage, driving out moisture and neutralizing trapped charges, it is obvious to a person skilled in the art to conduct this heat treatment in the manufacturing process of D1. Suitable temperatures and durations for this treatment would be arrived at by straightforward experimentation falling within the competence of the skilled person.

6.5 Accordingly, the subject-matter of claim 1 is obvious to the person skilled in the art and, thus, lacks an inventive step (Article 56 EPC 1973).

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar: Chair:

S. Sánchez Chiquero G. Eliasson