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Datasheet for the decision of 4 November 2014

Case Number: T 2189/09 - 3.4.03

Application Number: 99307990.4

Publication Number: 0994508

IPC: H01L23/485, H01L21/60

Language of the proceedings: EN

Title of invention:
Semiconductor device comprising bump contacts

Applicant:
SHINKO ELECTRIC INDUSTRIES CO. LTD.

Headword:

Relevant legal provisions:
EPC 1973 Art. 54, 56

Keyword:
Novelty - main request (yes)
Inventive step - main request (yes)

Decisions cited:

Catchword:

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Case Number: T 2189/09 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 4 November 2014

Appellant: (Applicant)	SHINKO ELECTRIC INDUSTRIES CO. LTD. 711, Aza Shariden, Oaza Kurita Nagano-shi, Nagano 380-0921 (JP)
Representative:	Finnie, Peter John Gill Jennings & Every LLP The Broadgate Tower 20 Primrose Street London EC2A 2ES (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 4 May 2009 refusing European patent application No. 99307990.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	V. L. P. Frank
	T. Bokor

Summary of Facts and Submissions

I. This is an appeal against the refusal of European patent application No. 99 307 990 for lack of novelty.

II. As final requests on appeal the appellant requested at the oral proceedings that the decision under appeal be set aside and a patent be granted on the basis of claims 1-3 as filed in the oral proceedings before the board, as main request, or, alternatively, on the basis of claims 1-5 as filed with the letter dated 3 October 2014, as auxiliary request.

III. Claim 1 of the main request reads as follows:

"1. A process for manufacturing a semiconductor device, the process comprising the following steps of:
covering an active surface of a semiconductor chip (10) having electrodes with an insulating layer (100) having perforations at positions directly above the electrodes;
forming rewiring circuits (120) on the insulating layer (100) so that each rewiring circuit (120) provides electrical connection between an electrode of the semiconductor chip (10) in the bottom of a said perforation and an outer bump;
forming a conductive pad (122) formed as a part of each rewiring circuit (120) at a peripheral portion of each rewiring circuit;
attaching an insulating film (160) to the rewiring circuit (12) and a surface of the insulating layer (100) at a peripheral portion of the rewiring circuit (120), the insulating film (160) having through holes (180) so that the conductive pads (122) are exposed in the through holes (180); and

superimposing the outer bump (200) on the conductive pad (122) in a respective through hole so as to project to an outside opposite to the semiconductor chip (10), wherein the semiconductor chip electrodes are arranged at a small pitch and wherein the outer bumps are arranged at a large pitch in a matrix manner."

Claims 2 and 3 are dependent on claim 1.

The claims of the auxiliary request are of no relevance for this decision.

IV. The following document is mentioned in this decision:

D2 = DE 40 25 622 A

V. The examining division essentially argued that:

- Document D2 disclosed a contact bump for a semiconductor device, in particular, an integrated circuit. Integrated circuits comprised a large number of semiconductor devices having doped regions provided with electrodes (contacts). The electrodes were interconnected ("integrated circuit") via at least one electrically conducting layer or wiring level. The wiring level was separated from the active semiconductor surface by an insulating layer which had perforations or vias over the electrodes in order to establish electrical contacts between the wiring level (ie the rewiring circuit of the claim) and the electrodes. These features were thus implicit in the semiconductor device of D2. At the time of the filing of D2 the dimensions of the semiconductor elements were substantially smaller than the

dimensions of the conductor pads which connected the integrated circuit to the exterior (micrometer range and tenth of micrometer range, respectively). Moreover not every electrode required a single corresponding conductive pad for the connection to the exterior due to the interconnection of the semiconductor elements. D2 thus implicitly disclosed the claimed small pitch and large pitch of the electrodes and the bumps, respectively. An integrated circuit required furthermore at least two connections from the exterior to the (interconnected) semiconductor elements. The semiconductor device of D2 comprised thus at least two bumps which were arranged in a matrix manner (ie the smallest possible matrix of two points).

- Hence document D2 disclosed either explicitly or implicitly all the features of the semiconductor device of claim 1.

VI. The appellant argued in essentially as follows:

- The technical problem solved by the present application was to remove the need for a sub-circuit board replacing it by rewiring circuits and an insulating film. Generally, a sub-circuit board had at one side a large pitch arrangement to connect it to a main circuit board and at the other side a small pitch arrangement to connect it to the semiconductor chip. The use of the rewiring circuits allowed for a large pitch arrangement of the outer bumps and a small pitch arrangement of the electrodes without requiring a bulky and expensive sub-circuit board which had to be attached to the semiconductor device by an

"underfiller". The greater pitch (spacing) of the outer bumps in comparison with the electrodes on the semiconductor chip allowed for more substantial and reliable electrical connections, thereby reducing the possibility of problems during fabrication and use.

- The method of claim 1 required that the insulating film be attached to a surface of the insulating layer. The insulating film could thus not be equated with an insulating layer grown on an integrated circuit, but was a separate film which was attached with an adhesive to the insulating layer.

Reasons for the Decision

1. The appeal is admissible.

2. Main request - Novelty (Article 54 EPC 1973)

2.1 Document D2 discloses a method for forming a contact bump (*"Anschlußkontakthöker"*) 6, 7 on an aluminum wiring layer (*"Leiterbahn"*) 2 of a semiconductor circuit. Insulating layers (*"Isolationsschicht"*) 3, 5 extend over the semiconductor substrate 1 and the wiring layer 2. The insulating layers are removed in a contact region of the wiring layer so that electric contact between the bump and the wiring layer may be made (cf D2, Figures 1 and 2; column 1, lines 55 - 64).

2.2 The examining division argued that, since D2 explicitly mentioned that the disclosed contact bump might be used in particular in a conventional integrated circuit (cf

D2, claim 1), all the features of such a circuit were implicitly disclosed in D2. Hence the rewiring circuits of the claim could be equated to the metallization layers found in an integrated circuit which connected the electrodes of the transistors formed on the active surface of the semiconductor to each other and to the contact pads on the exterior surface of the semiconductor chip. Insulating layers were used in an integrated circuit to isolate the metallization layers from each other and from the active surface of the semiconductor. Moreover, since the electrodes of the transistors on the active surface of the semiconductor had a much smaller pitch than the exterior contacts of the semiconductor chip, the requirement that the rewiring circuits provided electric contact between electrodes having a small pitch and the outer bumps having a large pitch was met.

2.3 In the process of claim 1 of the main request a distinction is made between the insulating layer 100 and the insulating film 160 in that not only different names are used for them (ie layer and film, respectively) but also by the step of *"**attaching** an insulating film (160) to the rewiring circuit".* Hence the insulating film 160 has to be a free-standing film that is attached to the semiconductor chip eg via an adhesive. This is in agreement with the corresponding part of the description where it is stated that *"The insulation film 160 may be a film of polyimide resin coated on the back surface with an insulating adhesive"* (page 6, lines 21-23). Thus the insulating film 160 is neither grown nor deposited on a semiconductor chip as is usually done with the insulating layers of a conventional integrated circuit.

2.4 Hence the process of claim 1 differs from the explicit and implicit disclosures of document D2 in that a separate insulating film is attached to the rewiring circuit and a surface of the insulating layer at a peripheral portion of the rewiring circuit. The process of claim 1 is therefore new.

3. Main request - Inventive step (Article 56 EPC 1973)

3.1 From the previous discussion on novelty it follows that in the process of claim 1, the rewiring circuits cannot be equated to the internal metallization layers of a conventional integrated circuit, since they have to be formed at least in part on the insulating layer covering the outer surface of the semiconductor chip, so that the separate insulating film may be attached to the rewiring circuit. The rewiring circuits thus provide the electrical connection between the outer bumps and the electrodes on the semiconductor chip's outer surface and are protected from short-circuits by the insulating film. According to the description, they replace the conventional sub-circuit boards used for that purpose in the prior art.

3.2 The objective technical problem can thus be considered as how to provide an improved interconnection mechanism between a semiconductor chip and the connection terminals of a main circuit board (cf page 2, line 34 - page 3, line 8).

3.3 The claimed manufacturing process renders the use of the conventional sub-circuit board unnecessary, which in the prior art was used for contacting the semiconductor chip on one of its sides and the connection terminals on its other side, providing an electric connection between the small pitched

electrodes on the semiconductor chip's surface and the larger pitched connection terminals (cf Figure 14; page 1, line 10 - page 2, line 33).

3.4 Neither document D2 nor the other documents of the prior art cited in the European Search Report suggest forming rewiring circuits on the semiconductor chip, attaching an insulating film on them and superimposing outer bumps in the through holes formed in the insulating film so as to contact the conductive pads of the rewiring circuits.

3.5 The board judges for these reasons that the manufacturing process of claim 1 involves an inventive step within the meaning of Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside

2. The case is remitted to the department of first instance with the order to grant a patent with the following documents:

Description:

pages 1, 2, 6-12 as originally filed
pages 3, 5 as filed with the letter dated 19 September 2007
page 4 as filed in the oral proceedings before the board.

Claims:

1-3 as filed in the oral proceedings before the board.

Drawings:

Sheets 1/7-7/7 as originally filed

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated