Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 25 September 2013

Case Number: T 2058/09 - 3.5.02

Application Number: 98308979.8

Publication Number: 917295

IPC: H03M 13/00

Language of the proceedings: EN

Title of invention:
Mac processor with efficient viterbi acs operation and automatic traceback store

Applicant:
Lucent Technologies Inc.

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - no (all requests)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 2058/09 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 25 September 2013

Appellant: (Applicant)
Lucent Technologies Inc.
600 Mountain Avenue
Murray Hill, NJ 07974-0636 (US)

Representative:
Williams, David John
Page White & Farrer
Bedford House
John Street
London WC1N 2BF (GB)

Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 6 April 2009 refusing European patent application No. 98308979.8 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: M. Ruggiu
Members: R. Lord
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal of the applicant against the decision of the examining division to refuse European patent application No. 98 308 979.8. The reasons given for the refusal were that the subject-matter of the independent claims did not involve an inventive step (Article 56 EPC) and that the claims did not meet the requirements for clarity and support in the description of Article 84 EPC. This decision was based on the set of claims filed with letter dated 7 January 2009.

II. The following documents of the state of the art are relevant for this decision:

D1: US 5 375 129 A;
D3: US 5 633 897 A; and
D4: EP 0 700 164 A1.

III. In a communication accompanying a summons to oral proceedings, dated 24 June 2013, the board informed the appellant *inter alia* of its preliminary opinion that the subject-matter of the independent claims which were the subject of the decision under appeal (which form the basis of the current main request) did not involve an inventive step.

The appellant requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of the claims of the main request, or on the basis of the claims of one of the first, second or third auxiliary requests, all filed with letter dated 23 August 2013.

Oral proceedings before the board took place on 25 September 2013, at which the appellant was not represented, as previously indicated by letter dated 23 September 2013.

IV. Claim 1 according to the appellant's main request reads as follows:

"An arithmetic logic circuit (30) with automatic traceback bit store, comprising:

an add/subtract/compare unit (32) receiving a first data input (A) and a second data input (B), providing a data output (C), and comprising means to perform an operation on said data inputs in response to a plurality of control signals (42), the operation being selectable between an addition operation, a subtraction operation, and a compare operation;

said add/subtract/compare unit being further configured to generate a traceback bit at a traceback output (78) of the add/subtract/compare unit, the traceback bit having a value dependent on a result of the compare operation performed by said means to perform an operation;

a controllable traceback shift register (46) having a traceback bit input coupled to said traceback output of the add/subtract/compare unit and a control input for receiving a shift enable signal; and

a logic circuit (79) configured to generate the shift enable signal for application to the control input of the controllable shift register;

CHARACTERIZED BY:

said add/subtract/compare unit comprising a traceback bit generator (69) configured to generate the traceback bit as a function of a sign signal (68)

resulting from performance of the compare operation and a compare min/max mode signal (75) indicating if the compare operation outputs a minimum value or a maximum value of a given set of compared values;

said logic circuit receiving as a first one of its inputs a traceback mode signal (77) indicating that the add/subtract/compare unit is operating in a mode that requires generation and storage of the traceback bit and receiving as a second one of its inputs a compare signal (74) indicating that said compare operation is currently selected for performance from among the selectable addition, subtraction and compare operations, wherein said traceback bit is shifted into said traceback shift register when said traceback mode signal is active and said compare operation is performed."

Claim 8 according to the appellant's main request reads as follows:

"A method of performing a compare operation and concurrently storing a traceback bit CHARACTERIZED BY the steps of:

(a) providing a compare min/max mode signal (75) indicating whether the compare operation should return a minimum value or a maximum value of a given set of compared values;

(b) providing a first path metric value (60) and a second path metric value (62);

(c) subtracting said second path metric value from said first path metric value to determine a difference and a sign signal (68), said sign signal being active when said difference is less than zero and inactive when said difference is greater than or equal to zero;

(d) logically combining said sign signal with said compare min/max mode signal to generate a traceback bit (78);

(e) selecting one of said first path metric or said second path metric according to the value of said traceback bit;

(f) outputting said selected path metric as the result of said compare operation; and

(g) shifting said traceback bit into a traceback shift register (46); and

(h) providing a traceback mode signal (77) indicating that said traceback bit is to be generated, said step of shifting occurring responsive to said traceback mode signal being active."

Claim 1 according to the appellant's first auxiliary request differs from that of the main request in that in the opening paragraph of the claim the phrase "capable of carrying out at least a Viterbi add-compare-select operation" is inserted after the expression "traceback bit store".

Similarly claim 8 according to the appellant's first auxiliary request differs from that of the main request in that in the opening paragraph of the claim the phrase "of a Viterbi add-compare-select operation" is inserted after the expression "compare operation".

Claim 1 according to the appellant's second auxiliary request differs from that of the first auxiliary request by the addition at the end of the claim of the following text:

"and wherein responsive to:

said logic circuit receiving at said first input said traceback mode signal indicating that the add/subtract/compare unit is operating in said mode that requires generation and storage of the traceback bit; and

said logic circuit receiving at said second input said compare signal indicating that said compare operation is currently selected for performance,

shifting said traceback bit into said traceback shift register and performing said compare operation in a same machine cycle of said arithmetic logic circuit".

Claim 8 according to the appellant's second auxiliary request differs from that of the first auxiliary request by the addition at the end of the opening paragraph (after "traceback bit") of the phrase "in an arithmetic logic circuit (30)", by the addition to the end of feature (g) of the phrase "of said arithmetic logic circuit", and by the amendment of feature (h) to read:

"(h) providing a traceback mode signal (77) indicating that said traceback bit is to be generated, said step of shifting occurring responsive to:

said traceback mode signal being active; and

a compare signal (74) being active, said compare signal indicating that a compare operation is currently selected for performance from among selective addition, subtraction and compare operations of an add/subtract compare unit (32) of said arithmetic logic circuit; and

wherein said compare operation and said shifting said traceback bit into said traceback shift register

are performed in a same machine cycle of said arithmetic logic circuit".

Claim 1 according to the appellant's third auxiliary request differs from that of the second auxiliary request by the addition at the end of the claim of the following text:

"and wherein said add/subtract/compare unit is further configured to perform at least one of an addition operation and a subtraction operation which is not associated with a Viterbi add-compare-select operation".

Claim 8 according to the appellant's third auxiliary request differs from that of the first auxiliary request by the addition at the end of the opening paragraph (after "traceback bit") of the phrase "in the arithmetic logic circuit of claim 1", by the replacement of the indefinite article "a" in each of features (g) and (h) by "said", and by the deletion of the reference number "(46)" in feature (g).

V. The appellant essentially argued as follows:

In their argument concerning inventive step in the decision under appeal the examining division provided no evidence for the allegation that the option of providing the possibility of selecting the minimum value in the compare step would be obvious to the skilled person.

The claimed method and apparatus provided the advantages over the prior art Texas Instruments DSP

devices described in paragraphs [0013] and [0014] of the published application.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request - Inventive step (Article 56 EPC)*

2.1 Since the independent method claim 8 of the main request has a broader scope than the independent apparatus claim 1, this claim will be considered first for the assessment of inventive step. It has not been disputed that the method described in document D1 with reference to Fig. 7 (noting that the indication "TO TRACE BACK SECTION" at the bottom right of that figure is understood as a reference to the right-hand section of the apparatus depicted in Fig. 2) comprises all the technical features of claim 8 of the appellant's main request other than features (a), (d) and (h).

2.1.1 Concerning the last of these features, the board considers it to be implicit in D1 that control signals must be provided to ensure that each part of the apparatus carries out the described process steps, and that the signal controlling the elements 27 ("SUBTRACT") and 30 ("SHIFT REGISTER") in Figs. 2 and 7 can be considered as a traceback mode signal within the meaning of feature (h) of this claim.

2.1.2 Features (a) and (d) of the claim thus represent the only distinguishing features with respect to the method of D1. They both relate to the provision of the

alternative modes of operation by which the compare step can select either the minimum or the maximum of the two compared values, whereas D1 describes only the selection of the maximum value. The board considers that the skilled person would be aware of the alternative mode of operation in which the compare step selects the minimum value, this being illustrated by documents D3 and D4, which like the present application describe dual-MAC circuits and methods for carrying out the Viterbi add-compare-select (ACS) operation, and which provide the minimum value as the output of the compare step (see in particular D3, column 6, line 54 to column 7, line 17 and Fig. 2, and D4, page 8, lines 50 to 57, page 11, line 36 to page 12, line 42 and Fig. 14). Since all three of these cited documents are concerned with providing increased circuit flexibility (see in particular D1, paragraph spanning columns 17 and 18, D3, column 7, lines 18 to 25 and D4, page 11, lines 16 to 25), the board considers that it would be obvious to the skilled person to increase the flexibility of the method of D1 by providing both options for the compare operation in a single processor, in order for instance to accommodate different logic computation conventions. The provision of an appropriate control signal to select between these two options (the compare min/max signal in the terminology of the present application) would then be trivial. The board therefore concludes that the subject-matter of the independent claim 8 of the appellant's main request does not involve an inventive step within the meaning of Article 56 EPC.

2.2 The independent apparatus claim 1 of the main request defines apparatus features corresponding to the method

features of claim 8 as discussed above, and additionally specifies that the subtract function in the compare step is carried out by one of the add/subtract/compare units which also carry out the addition function in the generation of the path metrics, signals (traceback mode signal and compare signal) being provided to control this function.

2.2.1 This additional feature represents the only significant further distinguishing feature of claim 1 with respect to D1 beyond that discussed above with respect to claim 8, since the apparatus of D1 (like those of D3 and D4) includes a separate subtractor unit for the subtract function of the compare step (see e.g. element 27 in Fig. 7 of D1, element 50 in Fig. 2 of D3 and element "COMPAR" in Fig. 14 of D4). However, taking into account the fact that each of these documents is concerned with reducing the number of clock cycles required for the ACS operation (see for instance D1, paragraph spanning columns 12 and 13, D3, column 1, lines 55 to 60 and D4, page 11, lines 7 to 15), the board is of the opinion that the provision of a separate subtractor in those documents can be seen as a deliberate choice, since this enables the adders to be freed to commence on the calculation of the next path metric while the compare step is being carried out. By contrast, in the arrangement defined in the present claim the calculation of the next path metric could not commence until the compare step was completed, and during this step the second add/subtract/compare unit would remain idle. The board therefore considers that these two alternatives represent merely a design trade-off between calculation speed and circuit complexity.

2.2.2 The further definitions in claim 1 relating to the traceback bit generator and the traceback shift register represent merely an obvious implementation of the traceback bit generation and storage which does not differ significantly from what is described in D1, D3 and D4, in particular given that, as noted above, these documents are also concerned with reducing the total number of clock cycles required for the ACS operation.

2.3 The only argument which the appellant has presented during the appeal procedure relating to the argumentation on inventive step based on document D1 concerned the fact that the argumentation in the decision under appeal did not cite any evidence for the knowledge of the skilled person relating to the alternative of providing the minimum value in the compare operation. This argument has been addressed by the citation of documents D3 and D4 in the above argumentation, to which the appellant has not responded. The remainder of the argumentation on inventive step in the statement of grounds of appeal (letter dated 17 August 2009) and in the reply to the summons to oral proceedings (letter dated 23 August 2013) concerned a comparison of the claimed invention with the prior art described in paragraphs [0013] and [0014] of the present application (this reference being to the published application). The appellant has not presented any arguments as to why that prior art and not D1 should be taken as the starting point for the assessment of inventive step. Indeed, since the description of that prior art in the application indicates that it does not include circuits for the automatic generation and storage of the traceback bit,

it seems to the board that it would be significantly less relevant than any of the documents D1, D3 and D4.

2.4 The board therefore concludes that the subject-matter of the independent claims 1 and 8 of the main request does not involve an inventive step according to Article 56 EPC.

3. *Auxiliary requests - Inventive step (Article 56 EPC)*

3.1 The independent claims of the first auxiliary request differ from those of the main request only in that the apparatus and method are specifically restricted to carrying out the Viterbi add-compare-select operation. Since each of the documents D1, D3 and D4 is concerned with processors for carrying out that operation, the conclusion of paragraph 2.4 above applies correspondingly to this request.

3.2 The independent claims of the second auxiliary request define the functioning of the traceback mode signal and the compare signal more precisely than in the main and first auxiliary requests, and additionally define that the shifting of the traceback bit into the traceback shift register and the performing of the compare operation are carried out in the same machine cycle of the apparatus. In the opinion of the board, the comments in paragraph 2.2.2 above apply also to these claims.

3.3 Independent claim 1 of the third auxiliary request differs from that of the second auxiliary request only in that it defines that the add/subtract/compare unit is further configured to perform at least one of an

addition operation and a subtraction operation which is not associated with a Viterbi add-compare-select operation. Since each of the documents D1, D3 and D4 discloses this feature (see the passages cited in paragraph 2.1.2 above in the context of increased circuit flexibility), this amendment cannot result in the presence of an inventive step. The independent method claim 8 additionally specifies that the method uses the circuit of claim 1, which amendment also cannot result in the presence of an inventive step, given the above conclusion relating to the apparatus claim.

3.4 The appellant has not presented any arguments as to why the amendments introduced in the three auxiliary requests might result in the presence of an inventive step. The board therefore concludes that the subject-matter of the independent claims of the first, second and third auxiliary requests does not involve an inventive step according to Article 56 EPC.

4. In the light of the above conclusions relating to inventive step for each of the appellant's requests, the appeal has to be dismissed. It is therefore also not necessary for the board to consider the issues relating to added subject-matter (Article 123(2) EPC) and clarity (Article 84 EPC) raised in the communication accompanying the summons to oral proceedings of 24 June 2013.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu