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Datasheet for the decision of 19 December 2012

Case Number: T 1927/09 - 3.5.02

Application Number: 04013448.8

Publication Number: 1487107

IPC: H03K 19/177

Language of the proceedings: EN

Title of invention:
Apparatus and methods for communicating with programmable logic devices

Applicant:
ALTERA CORPORATION

Headword:
-

Relevant legal provisions:
EPC Art. 123(2), 56, 111(1)

Keyword:
"Novelty -yes (after amendment)"
"Remittal"

Decisions cited:
-

Catchword:
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Case Number: T 1927/09 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 19 December 2012

Appellant: (Applicant)
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Representative:
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 30 March 2009 refusing European patent application No. 04013448.8 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: M. Ruggiu
Members: M. Rognoni
P. Mühlens

Summary of Facts and Submissions

I. The appellant (applicant) appealed against the decision of the examining division refusing European patent application no. 04 013 448.8.

II. In the decision under appeal, the examining division found, *inter alia*, that the subject-matter of claim 1 according to the main request and to the first, second and third auxiliary requests was not new with respect to the following document:

D1: US-A-5 794 033.

III. With the statement of grounds of appeal, the appellant requested to set aside the decision of the examining division and to grant a European patent on the basis of the main request or any one of the first to third auxiliary requests considered in the decision of the examining division.

IV. In a communication dated 5 October 2012 summoning the appellant to oral proceedings, the Board expressed the preliminary view that the circuit arrangement shown in Figure 7 of D1 appeared to read on to claim 1 of the appellant's main request and first auxiliary request. Hence, the Board shared the examining division's opinion relating to the lack of novelty of the subject-matter of these requests.

As to the second and third auxiliary requests, the Board noted that the wording which distinguished claim 1 of these requests from claim 1 of the main request related to subject-matter which was not

supported by the application as originally filed. Hence, these requests did not appear to comply with Article 123(2) EPC.

In the contested decision, the examining division had only considered the appellant's requests with respect to Article 54 EPC. However, in the light of the appellant's submissions relating to the patentability of the requests on file, the Board decided to address also the question of inventive step and, in particular, drew the appellant's attention to the following document:

D9: US-A1-2003/0023771.

Contrary to the appellant's view, expressed on page 7, last paragraph, of the statement of grounds of appeal, that there was no suitable hint in any of the cited documents which would prompt the skilled person to adapt the closest prior art to arrive at something falling within the terms of claim 1 and that therefore the subject-matter of claim 1 of all requests involved an inventive step, the Board concluded that, in the light of the teaching disclosed in D1 and of the skilled person's general knowledge, as summarized in D9, it seemed obvious to couple a PLD directly with a serial memory by means of a bi-directional serial interface.

V. In response to the Board's communication, the appellant filed with a letter dated 19 November 2012 a new main request and new first to third auxiliary requests, whereby claim 1 of the main request was essentially based on a combination of independent claim 1 of the

previous main request and of its dependent claims 12 and 14.

VI. In view of the appellant's new submissions dated 19 November 2012 and of the desire expressed by the appellant's representative in a telephone consultation with the rapporteur to receive some feedback prior to the oral proceedings scheduled for 19 December 2012, the rapporteur, by fax dated 17 December 2012, referred to the following prior art, which appeared to be relevant for a possible discussion on inventive step:

D10: WO-A1-96/35263

D11: "Secure Configuration of Field Programmable Gate Arrays" by Tom Kean; G.Brebner and R. Woods (Eds): FPL 2001, LNCS 2147, pp 142 - 151, 2001, © Springer-Verlag Berlin Heidelberg 2001

D12: US-A1-2001/0015919.

In particular, the rapporteur drew the appellant's attention to Figure 16 of D10, which showed a Master-Slave serial configuration of several field programmable gate arrays (FPGAs), and to D11 (section 3) and D12 ("Background of the Invention" and paragraph [0037]), which related to the use of Flash memories as storage devices for FPGAs.

VII. Oral proceedings were held before the Board on 19 December 2012.

VIII. The appellant requested that the decision under appeal be set aside and that the case be remitted to the

department of first instance for further prosecution on the basis of the claims of the main request or the first auxiliary request filed in the oral proceedings of 19 December 2012.

IX. Claim 1 of the main request reads as follows:

"A circuit arrangement, comprising:

a first programmable logic device (103A) comprising:

- a plurality of programmable logic blocks (112) of configurable logic circuitry;

- configuration circuitry (121) adapted to receive configuration information and to configure the plurality of programmable logic blocks (112);

a second programmable logic device (103B) comprising:

- a plurality of programmable logic blocks (112) of configurable logic circuitry; and

- configuration circuitry (121) adapted to receive configuration information and to configure the plurality of programmable logic blocks (112);

a storage device (106); and

a bi-directional serial interface (109; 109A) comprising:

- a serial data-out signal (SDO, 127) for providing data from storage device (106) to the first

programmable logic device (103A), the data comprising configuration information;

- a serial data-in signal (SDI, 130) for supplying data from the first programmable logic device (103A) to storage device (106);

- a serial clock signal (SCK, 133) for providing clock signals from the first programmable logic device (103A) to storage device (106); and

- a chip enable signal (CE*, 136),

wherein the storage device (106) is adapted to communicate the configuration information with the first programmable logic device (103A) and the second programmable logic device (103B) via the bi-directional serial interface (109; 109A),

wherein the second programmable logic device (103B) couples to the serial data-out signal and the serial clock signal in said bi-directional interface (109A), and

wherein the first programmable logic device (103A) is adapted to initiate its configuration by providing operation codes to the storage device (106) via said bi-directional serial interface (109; 109A), and to initiate the configuration of the second programmable logic device (103B) from the storage device (106) by asserting a chip enable signal to the second programmable logic device (103B)."

Claims 2 to 13 are directly or indirectly dependent on claim 1.

Claim 1 according to the first auxiliary request differs from claim 1 of the main request only in that the term "storage device" is replaced by the expression "serial Flash memory"

Claims 2 to 12 of the first auxiliary request are directly or indirectly dependent on claim 1.

X. The appellant's arguments relevant to the decision can be summarized as follows:

Although late-filed, the requests filed at the oral proceedings should be admitted into the appeal proceedings because their filing was prompted by the comments made by the Board in its communication to the appellant. Moreover, they overcame the novelty objection on which the refusal of the application was based. In fact, in the circuit arrangements disclosed in D1, the field programmable gate arrays following the lead FPGA were not directly connected to the serial bus, but received the configuration data from the preceding FPGA.

In view of the fact that the examining division had only considered the issue of novelty and that new documents D9 to D12 had been cited by the Board, it was appropriate to remit the case to the department of first instance for further prosecution.

Reasons for the decision

1. The appeal is admissible.

Admissibility of the appellant's requests

2.1 Claims 1 of all requests examined by the department of first instance and claims 1 of the requests filed with the statement of grounds of appeal are directed to a circuit arrangement comprising a *"programmable logic device"*, *"a storage device"* and *"a bi-directional serial interface"*. Embodiments of such circuit arrangement are illustrated in Figures 1 to 5.

2.2 Claims 1 of the main request and of the first auxiliary request now on file, which correspond essentially to the main and first auxiliary requests submitted with the letter dated 19 November 2012, relate to a circuit arrangement comprising *"a first programmable logic device"*, *"a second programmable logic device"*, *"a storage device"* and *"a bi-directional serial interface"*. Their subject-matter is essentially concerned with *"cascade-mode programming of PLDs"* (see paragraph [0057] of the application as published) and reflects the embodiment of the invention illustrated in Figure 9.

2.3 As to the admissibility of the main and the first auxiliary requests, the appellant has essentially argued that they aimed at defining the present invention in such a manner as to overcome the lack of novelty objection on which the refusal of the application was based.

2.4 The subject-matter for which protection is now sought differs considerably from the subject-matter of the previous independent claims, in the sense that it appears to shift the gist of the invention from the idea of providing a serial communication between a PLD and a serial memory by a means of a bi-directional serial interface to the idea of allowing one storage device connected to a bi-directional serial interface to program several PLDs in a sequential manner. However, the present requests are still concerned with the combination of a storage device with PLDs and a bi-directional serial interface and can thus be regarded as relating to a particular aspect of the invention (*i.e.* the loading of configuration data from the storage device into the PLDs), as disclosed in the original application.

2.5 In the result, the Board accepts that the present requests constitute a legitimate and reasonable attempt on the part of appellant to defend its application in the appeal procedure and thus decides to admit them into the proceedings in spite of their late filing (Article 13(1) RPBA).

Article 123(2) EPC

3.1 Claim 1 according to the main request is based on a combination of independent claim 1 of the main request considered in the contested decision and of its dependent claims 12 and 14. Furthermore, it specifies that the second programmable logic device couples to *"the serial data-out signal and the serial clock signal"* in the bi-directional interface. The wording *"by passing a signal*" used in dependent claim 14 has

been replaced by *"by asserting a chip enable signal*" in conformity with the wording used in the original application (cf. paragraph [0062] of the published application).

3.2 As pointed above (see item 2.2), the subject-matter of claim 1 reflects essentially the embodiment of the invention shown in Figure 9 and described in paragraphs [0057] to [0065] of the published application.

3.3 As to claim 1 of the first auxiliary request, it differs from claim 1 of the main request only in that the storage device is a *"serial FLASH memory*". This feature finds support, for instance, in paragraph [0061], lines 24 and 25, of the published application.

3.4 In summary, the Board finds that claims 1 of the main request and of the first auxiliary request do not contain subject-matter going beyond the content of the original application. Hence, they comply with Article 123(2) EPC.

Novelty

4.1 Claim 1 according to the main request relates to a circuit arrangement for cascade programming two programmable logic devices connected to a storage device via a bi-directional serial interface.

4.2 Figure 1 of D1 shows a circuit arrangement for loading, according to the "Master Serial Mode", a plurality of programmable logic devices 11, 12 and 13 with configuration data stored in a serial memory 10. As specified in column 2, lines 2 to 16, in "*this Master*

Serial Mode, the "Lead FPGA" generates control signals to drive the PROMs and it propagates the serial data to the "Slave FPGAs" connected in daisy chain mode. ... The Lead FPGA 11 also gives the CCLK clock 14 to the Slave FPGAs 12, 13 (and all Slave FPGAs not represented on the figure), and forwards configuration data to the DIN input of the first Slave FPGA 12 via its DOUT output. The same principle is used to forward configuration data from the first Slave FPGA 12 to the second Slave FPGA 13, and so on until the end of the daisy chain...".

In all the other circuit arrangements shown in Figures 2 to 5 and 7 of D1, the configuration data stored in the storage device are forwarded to a FPGA following the lead FPGA via the preceding FPGA in the daisy chain.

4.3 An essential difference between the circuit arrangement known from D1 and the subject-matter of claim 1 is that according to the latter the second programmable storage device obtains the data-out signal and the serial clock signal directly from the bi-directional interface and not via the preceding programmable storage device (see penultimate paragraph of claim 1), whilst configuration of the second programmable logic device with the configuration data stored in the storage device is initiated by the first programmable logic device (cf. last paragraph of claim 1).

4.4 The same configuration for programming two programmable storage devices is specified in claim 1 according to the first auxiliary request.

4.5 Thus, both the subject-matter of the main request and the subject-matter of the first auxiliary request are new with respect to D1 (Article 54 EPC).

Remittal to the department of first instance

5. In the contested decision, the examining division dealt only with the issue of novelty with respect to D1. In view of the fact that the subject-matter of the main and first auxiliary requests submitted to overcome the novelty objection is substantially different from the one of the claims considered by the examining division and, in fact, appears to be directed to the solution of a different problem, the Board considers it appropriate to make use of its power under Article 111(1) EPC and, in accordance with the appellant's request, to remit the case to the department of first instance for further prosecution.

Order

For the following reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution on the basis of the claims of the main request or the first auxiliary request filed in the oral proceedings of 19 December 2012.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu