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Datasheet for the decision of 10 December 2013

Case Number: T 1858/09 - 3.4.03

Application Number: 98963265.8

Publication Number: 1064679

IPC: H01L21/768

Language of the proceedings: EN

Title of invention:
PROCESS FOR FABRICATING AN INTEGRATED CIRCUIT WITH A SELF-ALIGNED CONTACT

Applicants:
ADVANCED MICRO DEVICES, INC.
FUJITSU LIMITED
Fujitsu AMD Semiconductor Limited

Headword:

Relevant legal provisions:
RPBA Art. 13(1), 13(3)
EPC Art. 123(2)
EPC 1973 Art. 56, 84
EPC 1973 R. 29(4)

Keyword:
Admission of main and auxiliary request (yes)
Added subject-matter (yes) - main request
Conciseness (no) - main request
Added subject-matter (yes) - auxiliary request
Inventive step (no) - auxiliary request

Decisions cited:

Catchword:

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Case Number: T 1858/09 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 10 December 2013

Appellants: (Applicants)

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Decision under appeal:

Decision of the Examining Division of the European Patent Office posted on 5 March 2009 refusing European patent application No. 98963265.8 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: R. Bekkering
T. Karamanli

Summary of Facts and Submissions

I. This is an appeal against the refusal of application No. 98 963 265 for lack of an inventive step, Article 56 EPC, and lack of support by the description, Article 84 EPC, for independent claim 6.

II. Oral proceedings were arranged as requested by the appellants. The summons to these oral proceedings was provided with an annex in which a provisional opinion of the board on the matter was given.

In the annex, it was noted that it appeared that the subject-matter of independent claims 1 and 6 lacked an inventive step, Article 56 EPC 1973, that claim 6 contained subject-matter extending beyond the content of the application as originally filed, Article 123(2) EPC, and that claim 6 should have been drafted as a dependent claim in conformity with Rule 29(4) EPC 1973.

III. In a letter dated 8 November 2013, in response to these summons, the appellants filed a new main and auxiliary request.

Moreover, the appellants announced that the applicants would not be represented at the oral proceedings.

Oral proceedings were held on 10 December 2013 in the absence of the appellants.

IV. The appellants requested in the letter dated 8 November 2013 that the decision under appeal be set aside and that a patent be granted on the basis of the following:

Main request:

Claims 1 to 10 filed with the letter of 8 November 2013,

Auxiliary request:

Claims 1 to 10 filed with the letter of 8 November 2013.

V. Claim 1 of the main request reads as follows:

"*A method of fabricating a contact for a transistor, the transistor having a gate (82, 14, 20), a source (16, 22), and a drain (12, 18), the method comprising:*
depositing an etch stop layer (40) over the gate (82, 14, 20), the drain (12, 18), and the source (16, 22);
depositing a first interlevel dielectric layer (64) over the etch stop layer (40);
first etching the first interlevel dielectric layer (64) from above the source (16, 22) and the drain (12, 18) to create first openings between adjacent gates over both source (16, 20) and drain (12, 18);
second etching the etch stop layer (40) from above the source (16, 22) and the drain (12, 18) to create second openings, smaller than the first openings, wherein the second openings expose the both drain (12, 18) and source (16, 22);
depositing a first conductive material over the gate (82, 14, 20) the source (16, 22) and the drain (12, 18), the first conductive material contacting each of said source (16, 22) and drain (12, 18),
planarizing the first conductive material to a first level approximate a second level (76) of the first interlevel dielectric layer (64), whereby plugs (50, 52) are simultaneously formed for each of drains (18, 20) and sources (16, 22);

depositing a second interlevel dielectric layer (66) above each plug (50, 52) and first interlevel dielectric layer (64);
third etching the second interlevel dielectric layer (66) to form a third opening above at least one of plug (50, 52); and
depositing a second conductive material over the second interlevel dielectric and the at least one plug, thereby filling the third opening with the second conductive material to form a contact (26) which is coupled to at least one of plug (50, 52) and to the drain (12, 18) or source (16, 22) through plug (50, 52), whereby the method allows the plug (50, 52) to overlap or butt against an adjacent gate, characterized in that,
the gate is a stacked gate which includes a floating gate and a control gate;
the first etching step etches the first interlevel dielectric layer from above the source (16, 22) and drain (12, 18) to retain an insulating layer of first interlevel dielectric layer (64) lying above the stacked gate, and the second etching step removes the etch stop layer (40) covering drain (12, 18) and sources (16, 22), whereby the stacked gate is insulated from the first conductive material by at least etch stop layer (40)."

Claim 6 of the main request reads as follows:

"*A method of fabricating a contact for a transistor, the transistor having a gate (82, 14, 20), a source (16, 22), and a drain (12, 18), the method comprising:*
depositing a first etch stop layer (42) over the gate (82, 14, 20), the drain (12, 18), and the source (16, 22), the first etch stop layer (42) comprising silicon oxide nitride (SiON);

etching the first etch stop layer (42) to leave an etch stop layer (42) on top of the gate (82, 14, 20);
depositing an insulating layer (38) to cover gates (82, 14, 20), source (16, 22), and drain (12, 18);
etching the insulating layer to form side wall spacer (38);
depositing a second etch stop layer (40) to cover a gate stack, source (16, 22) and drain (12, 18), where the gate stack comprises of a gate (82, 14, 20), etch stop layer (42) and side wall spacer (38);
depositing a first interlevel dielectric layer (64) over the second etch stop layer (40);
etching the first interlevel dielectric layer (64) to create a first opening above the source (16, 22) and the drain (12, 18);
etching the second etch stop layer (40) to create a second opening, smaller than the first opening, wherein the second opening exposes the source (16,22) and the drain (12, 18);
planarizing the first interlevel dielectric layer (64) to a second level (76);
depositing a first conductive material above the source (16, 22) and the drain (12, 18),
planarizing the first conductive material to a first level approximate a second level of the first interlevel dielectric layer (76), whereby plugs (50, 52) are simultaneously formed contacting drains (12, 18) and sources (16, 22);
depositing a second interlevel dielectric layer (66) above the [sic] *(50, 52) and the first interlevel dielectric layer (64);*
etching the second interlevel dielectric layer (66) to form at least one contact hole above the drain (12, 18) and/or source (16, 22); and
filling the at least one contact hole with a second conductive material to form plug (26, 28) coupled to

the drain (12, 18) and/or source through plug (50, 52), whereby the method allows the plug (50, 52) to overlap or butt against an adjacent gate (82, 14, 16), characterized in that, the adjacent gate is a stacked gate that includes a floating gate and a control gate; and that is insulated from the plug (50, 52) by a side wall spacer (38)."

VI. Claim 1 of the auxiliary request corresponds to claim 1 of the main request.

Claim 6 of the auxiliary request reads as follows:

"*The method of claim 1 further comprising:*
depositing a first etch stop layer (42) over the gate (82, 14, 20), the drain (12, 18), and the source (16, 22), the first etch stop layer (42) comprising silicon oxide nitride (SiON), before depositing said etch stop layer;
etching the first etch stop layer (42) to leave an etch stop layer (42) on top of the gate (82, 14, 20);
depositing an insulating layer (38) to cover gates (82, 14, 20), source (16, 22), and drain (12, 18);
etching the insulating layer to form side wall spacer (38);
then depositing said etch stop layer (40) to cover the gate stack comprising said gate (82, 14, 20), etch stop layer (42) and side wall spacer (38), and said source (16, 22) and drain (12, 18).
including the step of, following creations of said second opening, planarizing the first interlevel dielectric layer (64) to a second level (76);
and wherein said step of etching the second interlevel dielectric layer (66) forms at least one contact hole above the drain (12, 18) and/or source (16, 22); and

filling the at least one contact hole with a second conductive material to form plug (26, 28) coupled to the drain (12, 18) and/or source through plug (50, 52), and wherein the adjacent gate is insulated from the plug (50, 52) by a side wall spacer (38)."

VII. Reference is made to the following documents:

D1: US 5 668 052 A

D4: Kaanta C.W. et al., "*Dual Damascene: A ULSI Wiring Technology*", VLSI Multilevel Interconnection Conference Proceedings, 11 June 1991, pages 144 to 152

D10: US 5 598 028 A.

VIII. The appellants submitted in substance the following arguments:

The subject-matter of claim 1 according to the main request involved an inventive step. Document Dl never mentioned or even suggested that plugs contacting openings to both source and drain regions could be formed simultaneously. This addition provided a seventh concession of a difference with respect to document Dl over the six differences provided in the decision under appeal. The Dl method also required extra acts compared to the claimed method. The simultaneous formation of plugs contacting drains and sources provided an advantage as they could be made larger at their upper boundary without fear that such larger openings would interfere with nearby contact plugs. Moreover, precise alignment was not necessary. Document D4 was directed to a Double Damascene Process used to form multiple layers of metal interconnects above the substrate,

which was generally not suitable for making contact directly to doped regions of a substrate such as a source or drain region where polysilicon materials were often used. In document D10 no plugs were formed.

Claim 6 of the auxiliary request did not add matter to the application as filed. The application as filed set out that the first interlevel dielectric layer (64) was deposited over layer (42) [sic] and then planarised to level (76). Layer (64) was then etched to open apertures. Claim 1 stated that the first conductive material was planarised to a first level approximate a second level (76) of the first interlevel dielectric layer (64). While this did not explicitly state that the first interlevel dielectric layer (64) was planarised to the level (76), it nonetheless strongly implied it.

The subject-matter of claim 1 of the auxiliary request involved an inventive step for the same reasons given for the main request.

Reasons for the Decision

1. The appeal is admissible.

2. *Procedural issues*

The amended new claims according to the appellants' main and first auxiliary request were filed after oral proceedings before the board were arranged.

In view of the fact that the amendments were filed in advance of the oral proceedings, constitute an attempt to overcome the objections raised by the board and are provided with reasons in support thereof, and as the board is able to deal with the requests in substance, without adjournment of the oral proceedings, the new requests are admitted into the proceedings (Article 13(1) and (3) RPBA).

However, an appellant filing amendments, but renouncing to come to oral proceedings before the board to which it was duly summoned, must be taken to waive its right under Article 113(1) EPC 1973 to present comments on any ground for an adverse decision which may arise (Article 15(3) RPBA).

3. *Main request*

3.1 *Amendments*

As noted in the annex to the summons to the oral proceedings, and as acknowledged by the appellants in their letter of reply, according to the application as originally filed the step of planarizing the first interlevel dielectric layer 64 to a level 76 takes place before etching the layers 40 and 64 to open apertures or vias to the drain 12 and sources 16 and 22 (cf page 5, lines 19 to 24).

In contrast hereto, claim 6 defines, as the seventh and eight method step, etching the first interlevel dielectric layer (64) to create a first opening above the source (16, 22) and the drain (12, 18), and etching the second etch stop layer (40) to create a second opening, smaller than the first opening, wherein the second opening exposes the source (16, 22) and the

drain (12, 18), and only thereafter as the ninth method step, planarizing the first interlevel dielectric layer (64) to a second level (76).

The appellants argued (for the auxiliary request) that the application as filed at page 5, lines 19 to 21, set out that the first interlevel dielectric layer (64) was deposited over layer (42) [sic] and then planarised to level (76). Layer (64) was then etched to open apertures (page 5, lines 21 to 24). Claim 1 stated that the first conductive material was planarised to a first level approximate a second level (76) of the first interlevel dielectric layer (64). While this did not explicitly state that first interlevel dielectric layer (64) was planarised to the level (76), it nonetheless strongly implied it. Accordingly, claim 6 did not add matter to the application as filed.

The appellants' arguments above, however, while acknowledging that according to the description planarization takes place before etching the openings, do not address the issue that claim 6 as amended defines a planarization step after etching the openings and, thus, are not convincing.

Accordingly, claim 6 contains subject-matter, which extends beyond the content of the application as originally filed, contrary to the requirement of Article 123(2) EPC.

3.2 *Conciseness*

According to Article 84 EPC 1973, the claims shall be clear and concise. Moreover, according to Rule 29(4) EPC 1973, any claim, which includes all the features of any other claim, shall contain a reference to the other

claim and then state the additional features which it is desired to protect.

Claim 6 includes all the features of claim 1. Since claim 6 is not drafted as a dependent claim, it is not in conformity with Rule 29(4) EPC 1973 and not clear and concise, contrary to the requirements of Article 84 EPC 1973.

3.3 The appellants' main request is, therefore, not allowable.

4. *Auxiliary request*

4.1 *Amendments*

As noted above for the main request, according to the application as originally filed the step of planarizing the first interlevel dielectric layer 64 to a level 76 takes place before etching the layers 40 and 64 to open apertures or vias to the drain 12 and sources 16 and 22 (cf page 5, lines 19 to 24).

In contrast hereto, claim 6 defines that the method includes the step of, following creations [sic] of said second opening (exposing the drain and source (cf claim 1)), planarizing the first interlevel dielectric layer (64) to a second level (76).

Claim 6 thus contains subject-matter, which extends beyond the content of the application as originally filed, contrary to the requirement of Article 123(2) EPC.

4.2 *Novelty*

4.2.1 *Document D1*

Document D1 relates to the formation of a contact using a self-alignment scheme in the manufacturing of a semiconductor device.

In particular, D1 discloses, using the terminology of claim 1, a method of fabricating a contact for a transistor, the transistor having a gate (16), a source and a drain, the method comprising:

depositing an etch stop layer (20) over the gate and the source/drain (cf column 5, lines 23 to 28; figure 4);

depositing a first interlevel dielectric layer (21) over the etch stop layer (20) (cf column 5, lines 28 to 33; figure 4);

first etching the first interlevel dielectric layer (21) from above the source/drain to create first openings between adjacent gates over the source/drain (cf column 5, lines 60 to 65; figure 6);

second etching the etch stop layer (20) from above the source/drain, to create second openings, smaller than the first openings, wherein the second openings expose the source/drain (cf column 5, line 67 to column 6, line 34; figures 8 and 9);

depositing a first conductive material over the source/drain, the first conductive material contacting the source/drain, whereby a plug (22) is formed for the source/drain (cf column 6, lines 35 to 39; figure 1);

whereby

the method allows the plug (22) to overlap or butt against an adjacent gate (16) (cf column 5, lines 49 to 55; figures 1 and 5), and

wherein

the first etching step etches the first interlevel dielectric layer (21) from above the source/drain to retain an insulating layer of first interlevel dielectric layer (21) lying above the gate, and the second etching step removes the etch stop layer (20) covering the source/drain, whereby the gate (16) is insulated from the first conductive material (22) by at least etch stop layer (20) (cf column 5, line 60 to column 6, line 34; figures 1, 6, 8 and 9).

4.2.2 It is noted that document D1 only shows a contact formed to one of the source/drain regions of the transistor. Moreover, document D1 is silent on the specific steps taken to form the conductive plug (22) and the upper wiring layer (23) (cf column 6, lines 35 to 39; figure 1).

In particular, the claimed method differs from the method of document D1 in that:

1. the gate is a stacked gate, which includes a floating gate and a control gate;

2. contacts are made to both the source and drain of the transistor; and it includes

3. planarizing the first conductive material, deposited over the gate, source and drain, to a first level approximate a second level of the

first interlevel dielectric layer, whereby plugs are simultaneously formed for each of the drains and sources;

4. depositing a second interlevel dielectric layer above each plug and first interlevel dielectric layer (64);

5. third etching the second interlevel dielectric layer to form a third opening above at least one of plug (50, 52); and

6. depositing a second conductive material over the second interlevel dielectric and the at least one plug, thereby filling the third opening with the second conductive material to form a contact which is coupled to at least one of the plugs and to the drain or source through the plug.

4.2.3 Accordingly, the subject-matter of claim 1 is new over document D1, Article 54(1) EPC 1973.

The subject-matter of claim 1 is also new over the remaining, more remote prior art provided by documents D4 and D10.

4.3 *Inventive step*

4.3.1 There is no technical effect achieved by all the distinguishing features above taken in combination. Rather partial problems are independently solved by different sets of distinguishing features. As is in substance held in the decision under appeal, distinguishing features 1 to 6 identified above address the following partial problems to be solved relative to D1:

1a. Regarding distinguishing features 1 and 2, investigating the suitability of the Dl process of making a memory with self-aligned contact for the fabrication of further memory devices with self-aligned contacts to both the source and drain.

1b. Regarding distinguishing feature 3, the realization of the Dl plug (22) fabrication process.

1c. Regarding distinguishing features 4 to 6, the realization of a second conductive layer (23) process.

4.3.2 Regarding the above first partial problem to be solved 1a, it would be readily apparent to a person skilled in the art that the method of self-aligned contact formation of D1, providing the advantage that in case of misalignment of the contact opening a short circuit between the contact and the gate is prevented, is clearly also suitable for other known memory devices, notably those with a stacked gate and where contacts are formed to both the drain and the source such as shown in document D10 (cf figures 1A to 5A, 7, 9 and corresponding description). Accordingly, the solution as claimed to problem 1a is considered to be rendered obvious by document D10, showing the provision of contacts to both the drain and the source of a device with a stacked gate such as eg a flash memory device.

The solution as claimed to problems 1b and 1c is considered to be rendered obvious by document D4, showing a dual damascene process for forming studs (plugs).

In particular, regarding problem 1b, document D4 shows a dual damascene process for forming plugs of conductive material including depositing the conductive material over the device followed by a planarization step (cf page 145, last paragraph to page 146, first paragraph; page 146, figures 2e and 2f). It would be obvious for a person skilled in the art to use such a clearly suitable process for forming the conductive plug (22) in D1.

Regarding problem 1c, document D4 shows a process for forming a further interconnect level. The process comprises the repetition of steps 1 to 9 as disclosed with reference to figure 2 for each interconnect level.

In particular, the process involves for the second level the steps of:
depositing a second interlevel dielectric layer above each plug and first interlevel dielectric layer (cf page 145, second paragraph; page 146, figure 2a);
etching the second interlevel dielectric layer to form an opening above at least one plug (cf page 145, third paragraph; page 146, figure 2a); and
depositing a second conductive material over the second interlevel dielectric and the at least one plug, thereby filling the opening with the second conductive material to form a contact which is coupled to at least one of the plugs (cf page 145, last paragraph to page 146, first paragraph; page 146, figures 2e and 2f).

It would be obvious to a person skilled in the art to use the process suggested in document D4 to form the upper wiring layer (23) provided in the device of document D1.

Accordingly, the solution as claimed to problems 1b and 1c is considered to be rendered obvious by document D4.

4.3.3 According to the appellants, the Dl method required extra acts compared to the claimed method such as:

- forming an oxide film 19 in Fig. 4;
- forming a reflection prevention film 24 in Fig. 5;
- etching the reflection prevention film 24 in Fig. 6; and
- etching the oxide film 19 in Fig. 9.

Moreover, the claimed invention simultaneously formed plugs contacting drains and sources, which was not suggested in D1 and provided an advantage, as they could be made larger at their upper boundary without fear that such larger openings would interfere with nearby contact plugs since all the openings for such plugs were formed by a single mask and etch step. Moreover, precise alignment was not necessary, as could be seen from figure 6 [sic] of the application, where contact 26 was formed only to one of plugs 50, 52 and contact 26 was not precisely aligned to the plug it contacted.

Moreover, document D4 was directed to a Double Damascene Process used to form multiple layers of metal interconnects above the substrate. Such a process was generally not suitable for making contact directly to doped regions of a substrate such as a source or drain region where polysilicon materials were often used.

In document D10, as shown in figure 6 [sic], no plugs were formed, rather, the uniform contact openings were filled with a conductive material, which was then patterned to form conductive traces. This made it

impossible to separately form contacts to source and drain openings in a manner that would provide the optimum spacing and layout provided by the application.

4.3.4 Regarding the extra acts argued by the appellants, it is noted that claim 1 does not exclude the provision and/or removal of further layers such as a further underlying oxide layer and a reflection prevention layer. Moreover, it is noted that D1 also includes an embodiment in which no oxide film underlying the etching stopper film 20 is provided (see embodiment 3, column 7, line 65 ff. and figures 13 to 16). Regarding the reflection prevention film 24, it is noted that the skilled person would understand this layer to be required where reflection is an issue and thus omit the layer if it is not needed.

As to the appellants' argument that the claimed invention simultaneously formed drain and source contacts, it is noted that in D10 metal interconnection layer 17 (cf column 5, lines 13 to 57; figures 6 to 9) simultaneously forms a drain and a source contact, so that this feature would be obvious to the person skilled in the art. The advantages in terms of no risk of interference between nearby contacts are thereby provided as well. As to the argument that in D10 no plugs were formed, it is noted that the formation of plugs is already suggested in document D1.

As to the argued advantage that precise alignment was not necessary (cf figure 2 of the application, where contact 26 is not precisely aligned to the plug (50) it contacts), it is noted that the same advantage is provided in D1, where, as would be readily apparent to the skilled person, precise alignment of contact (23)

to conductive plug (22) is not necessary (cf D1, figure 1).

Finally, regarding document D4 it is noted that, whereas it is true that D4 concerns metal plugs and interconnects, it is not uncommon to form metal contacts to source and drain regions, see eg document D10, so that the skilled person would consider document D4 for a solution to the problem of realising plugs to the source and drain.

4.3.5 Accordingly, the subject-matter of claim 1 of the auxiliary request, having regard to the state of the art, is obvious to a person skilled in the art and, therefore, lacks an inventive step, Article 56 EPC 1973.

4.4 The appellants' auxiliary request is, thus, also not allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated