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**Datasheet for the decision
of 13 September 2013**

Case Number: T 1777/09 - 3.5.06

Application Number: 05776970.5

Publication Number: 1894114

IPC: G06F 13/40, G06F 13/376,
G06F 1/08, G06F 1/32

Language of the proceedings: EN

Title of invention:
Device and method for media access control

Applicant:
Freescale Semiconductor, Inc.

Headword:
Media access control/FREESCALE

Relevant legal provisions (EPC 1973):
EPC Art. 54(1,2), 111(1)

Keyword:
"Novelty - main request (yes)"
"Remittal to the department of first instance (yes)"

Decisions cited:
-

Catchword:
-



Case Number: T 1777/09 - 3.5.06

D E C I S I O N
of the Technical Board of Appeal 3.5.06
of 13 September 2013

Appellant:
(Applicant)

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Decision under appeal:

**Decision of the Examining Division of the
European Patent Office posted 15 July 2009
refusing European patent application
No. 05776970.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman: D. H. Rees
Members: A. Teale
W. Sekretaruk

Summary of Facts and Submissions

I. The appeal is against the decision by the examining division, dispatched on 15 July 2009, to refuse European patent application No. 05 776 970.5 on the basis that the subject-matter of claim 1 according to the then main request lacked novelty, Article 54(1,2) EPC 1973, in view of the document:

D5: The I²C-Bus specification, version 2.1, January 2000, 46 pages, XP002218697.

Amended claims according to an auxiliary request were not accepted at the oral proceedings before the examining division under Rule 137(3) EPC.

In the course of examination proceedings, the examining division also raised a novelty objection, Article 54(1,2) EPC 1973, in view of the following document:

D1: US 5 467 042 A.

II. Notice of appeal was filed and the appeal fee paid on 6 August 2009. Amended claims according to a main and first and second auxiliary requests were annexed.

III. The statement of grounds of the appeal was filed on 25 August 2009. The appellant requested that the appealed decision as a whole be set aside and that a patent be granted with the claims according to the main or first and second auxiliary requests. The appellant also requested oral proceedings in case rejection of any of its requests was intended.

IV. The enhanced electronic signature of both notice and grounds of appeal were corrected on 3 September 2009, in response to an invitation according to Rule 50(3) EPC.

V. The application documents currently on file are as follows:

Description (all requests):

Pages 1 to 30, as originally filed.

Claims (all received on 6 August 2009):

Main request: 1 to 21.

First auxiliary request: 1 to 21.

Second auxiliary request: 1 to 18.

Drawings (all requests):

Sheets 1 to 13, as originally filed.

VI. The set of claims according to the main request comprises independent claims 1, 12 and 21 and dependent claims 2 to 11 and 13 to 20. The independent claims read as follows:

"1. A method (100) for media access control, the method comprising generating (180) at least one media access grant in response to at least one media access request, the method characterized by: the media access controller: monitoring (130) the data line, while maintaining at least the clock line (440) in a low power mode, to detect the media access request generated by at least one component coupled to the data line (430) and to the clock line (440); and forcing

(140) the clock line (440) to exit the low power mode and starting a contention prevention period, when at least one component requests to access the data line (430) or when the media access controller determines to transmit information itself."

"12. A device (400, 400') comprising multiple components (420,410) coupled to a data line (430), characterized by the media access controller (410) being adapted: i) to monitor the data line, while maintaining at least a clock line in a low power mode, to detect at least one media access request for said data line generated by at least one of said components, (ii) to force the clock line to exit the low power mode and to start a contention prevention period, in response to at least one detected media access request or when the media access controller determines to transmit information itself, and (iii) to generate at least one media access grant."

"21. A computer readable medium (800) having stored thereon a set of instructions, the set of instructions, when executed by a media access controller (410), cause the media access controller (410) to generate at least one media access grant in response to at least one media access request; characterized by further causing the media access controller (410): (i) to monitor a data line (430), while maintaining at least a clock line (440) in a low power mode, to detect at least one media access request generated by at least one component coupled to the data line (430) and to the clock line; and (ii) to force the at least clock line to exit the low power mode and to start a contention prevention period, when at least one component requests

to access the data line or when the media access controller determines to transmit information itself."

Reasons for the Decision

1. *Admissibility of the appeal*

In view of the facts set out at points I to IV above, the appeal satisfies the admissibility criteria under the EPC and is therefore admissible.

2. *The context of the invention*

The application relates to controlling access by multiple components, such as individual integrated circuits, to a serial data bus in a power efficient manner. The bus comprises a data line and a clock line, some components connected to the bus acting as "masters" while the others act as "slaves". A master can send instructions and data to a slave, while a slave sends data or an interrupt request to a master. A media access controller executes stored instructions (see page 28, lines 7 to 11) and can act as a master on the bus, providing clock signals on the clock line during data transfers, in either direction, between the media access controller and another component connected to the bus. When the bus is free power consumption is reduced by reducing the clock speed on the clock line or by not providing a clock signal at all. The media access controller keeps the clock line in the low power mode while monitoring the data line to see if a component requests access to the data line to transmit data; see page 7, lines 7 to 13. Concerning the bus

protocol, figure 6 shows the bus information frame, in which a contention prevention bit (502) precedes *inter alia* synchronization bits, media access request bits, media access grant bits, destination address bits and data bits. A component asserts the data line to indicate to the media access controller that it requests access to the data line. Alternatively the media access controller may determine to transmit data over the data bus itself. In either case the contention prevention bit in the bus information frame defines a "contention prevention period" (see page 12, lines 11 to 24) which prevents simultaneous transmission by the media access controller and another component on the bus; see page 12, lines 4 to 10. Once the frame has been transmitted, the media access controller forces the components clocked by it to re-enter the low power mode.

3. *The amendments to the application*

3.1 Editorial amendments aside, claims 1, 12 and 21 according to the main request result from combining original claims 1, 14 and 38, respectively, with the expression "or when the media access controller determines to transmit information itself", based on page 7, lines 13 to 16. Claims 2 to 11 and 13 to 20 are the same as original claims 2 to 11 and 15 to 19, 9, 21 and 22, respectively.

3.2 The board is consequently satisfied that the amendments to the application comply with Article 123(2) EPC regarding added subject-matter.

4. *The construction of the claims*

Two expressions used in the claims require construction, namely "low power mode" and "contention prevention period".

4.1 *The expression "low power mode"*

4.1.1 The description mentions two examples for "low power mode". According to page 7, lines 7 to 13, "The media access controller 410 is capable of operating during low power modes when it does not provide a clock signal over the clock line 440. For example, it is capable of monitoring the data line 430 in order to determine whether one or more components out of multiple components 420 requests to transmit information over the data bus 430." In contrast, page 6, lines 24 to 31, discloses reducing power consumption by providing a low frequency clock signal in a low power mode.

4.1.2 The board considers that the expression in the claims "low power mode" is a clear generalisation of these two cases, hence supported by the description (Article 84 EPC 1973).

4.2 *The expression "contention prevention period"*

4.2.1 The description (see, for example, page 8, lines 1 to 10, and figure 9; step 140) discloses forcing "the at least clock line to exit the low power mode and start a contention prevention period, in response to at least one detected media access request or in response to a determination to transmit information by the media access controller itself". According to present

claims 9 and 18, the contention prevention period is one clock cycle long. According to page 11, lines 29 to 31, referring to figure 6, "The information frame 500 starts by a contention prevention bit 502 during which the media access controller 410 enters a high impedance state." According to page 12, lines 7 to 17, the contention prevention bit "prevents the simultaneous transmission by the media access controller 410 and a component out of components 420. Thus, during a contention prevention period that is defined by the contention prevention bit, the data line can convey a low value ("0") signal (if the data line 430 is successfully pulled down by pull down resistor 461), [or] convey a high value ("1") signal (if a component out of components 420 indicates that it requests to access the data line 430)."

- 4.2.2 The board considers that from the claimed subject-matter as a whole the skilled person would understand the expression in the claims "contention prevention period" to mean a period during which the media access controller monitors the data line to see whether any other bus component makes a media access request. This meaning is clear and again supported by the description.

5. *The prior art*

According to the reasons for the appealed decision, the subject-matter of claim 1 then on file lacked novelty, Article 54(1,2) EPC 1973, in view of D5. In the course of examination proceedings, the examining division also raised a novelty objection, Article 54(1,2) EPC 1973, in view of D1.

5.1 *Document D5*

5.1.1 D5 concerns the I²C-bus (Inter IC bus) used, for example, to connect a microcontroller with other devices such as LCD drivers and memory. The bus comprises a serial data line (SDA) and a serial clock line (SCL); see page 4, section 2, lines 28 and 29. Each device is connected to the SDA and SCL lines via an interface which, for instance, has open-drain outputs; see figure 3 on page 8. Depending on their logical state, such outputs either present a high impedance to the line or pull it down to the LOW state. Each bus line is bidirectional and connected via a current source or a pull-up resistor to V_{DD}, meaning that each bus line has a hard-wired AND function: the bus line can only be in the HIGH state (logical 1) if all devices allow it to go HIGH, any device being able to pull the bus line down to the LOW state (logical 0); see figure 3 and page 8, left paragraph, lines 8 to 13, and section 6. Data on the data line must be stable when the clock line is in the HIGH state, only changing when the clock line is in the LOW state: see figure 4 and page 8, section 6.1. There are only two exceptions to this rule: if the clock line is HIGH then a falling edge of the data line signifies a "Start" condition whilst a rising edge of the data line signifies a "Stop" condition; see page 9, figure 5. A "Start" condition causes all devices on the bus to reset their bus logic in anticipation of the sending of a slave address (see below).

5.1.2 Devices connected to the bus have a unique address and, irrespective of whether they transmit and/or receive data, can either act as a master or as a slave. A master initiates a data transfer on the bus and

generates the clock signals to permit that transfer; see page 6, section 4. Multiple masters can co-exist, collision detection and arbitration processes preventing data corruption if two or more masters simultaneously initiate data transfer. When the bus is free both the clock and data lines are HIGH and any master may start a transfer; see page 8, left column, lines 10 to 11. The process of arbitration ensures that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the "winning" message is not corrupted. During arbitration the first master to produce a 1 while another produces a 0 detects that, due to the wired AND function (see above), the bus data line is not following its data output and consequently it has "lost" the arbitration and must cease transmission; see page 7, right column, last seven lines, and page 12, right column, last paragraph. Eventually only one master is left as the "winner" of arbitration. During arbitration the wired AND function of the clock line combines the clock signals generated by the various active masters, termed clock "synchronization", to produce a composite clock signal in which the LOW period is determined by the master with the longest clock LOW period and the HIGH period is determined by the master with the shortest clock HIGH period; see page 11, section 8.1. As is stated on page 13, left column, lines 1 to 4, access to the bus is consequently decided by competition between the masters, there being no central master, nor any order of priority on the bus. The board understands that the outcome of arbitration is decided by the data that the various masters are seeking to transmit. A complete data transfer, shown on page 13 in figure 10, comprises a start condition, a 7-bit slave address, a read/write

bit, any number of 8-bit data bytes and their corresponding acknowledgments by the slave, and a stop condition; see also page 13, right column, last paragraph.

5.1.3 The I²C-bus specification has been extended since its inception; see section 11 on page 19. In particular, further possible maximum data transfer rates have been added beyond the initial "Standard-mode" of 100 kbit/s, namely "Fast-mode" (400 kbit/s) and "High-speed (Hs) mode" (3.4 Mbit/s). Fast-mode and Standard-mode use the same approach to arbitration and clock synchronization and are collectively referred to as "F/S-mode". The Hs-mode differs from F/S-mode in how arbitration is handled; see page 20, section 13, third sentence. In Hs-mode each master is allocated a predefined 8-bit "master code" which it transmits at F/S-mode speeds to achieve arbitration and clock synchronization before an Hs-mode data transfer occurs; see page 21, right column, lines 3 to 6. The board understands this to mean that in Hs-mode arbitration occurs according to master priorities determined by the master codes.

5.1.4 The appellant has disputed the findings in the appealed decision that the start condition known from D5 constitutes the claimed "media access request" and that D5 also discloses a "media access grant". The board is persuaded by the appellant's arguments. The system according to D5 can have multiple masters which, if no communication is occurring, can all create a "start condition" and start transmitting simultaneously. The start condition is however not a media access request in the meaning of the claims, since the masters simply start transmitting without first waiting to receive any

form of signal constituting a media access grant. In the F/S-mode, depending on the data competing masters try to transmit, only one master emerges as a "winner", the other masters simply ceasing to transmit data. Figure 9 on page 12 of D5 shows that, as soon as one transmitter (master 1 in the figure) detects that the actual level on the data line (SDA) is not the same as the internal data level (DATA 1) that it wants to transmit, it "backs off" and ceases to transmit, having "lost" arbitration. In the Hs-mode the competing masters try to transmit predetermined master codes. Also in this case the "losing" masters simply cease to transmit. In neither case do the competing masters wait for an access request to be granted by a media access controller before accessing the bus to transmit data.

5.1.5 According to the appellant, it follows from the fact that in D5 the winning master does not receive any signal granting it access to the medium that D5 does not disclose a media access controller. The appellant has also argued that claim 1 is limited to a centralized media access controller and pointed out that, according to D5, page 13, section 8.2, there is "no central master". The board does not agree that D5 does not disclose a media access controller for two reasons. Firstly, the board takes the view that the application does not provide a basis for construing claim 1 so narrowly that it excludes a distributed media access controller. Secondly, the way in which arbitration between competing masters occurs in D5 is a method of media access control, albeit in a distributed manner. Hence the device carrying out this method in D5 is necessarily a media access controller. The board however agrees with the appellant that D5 does not

disclose the plurality of masters (as a distributed media access controller) monitoring a data line while maintaining a clock line in a low power mode. There is no disclosure in D5 of the plurality of masters acting together to either stop the clock signal on the clock line (SCL) or to keep the clock frequency at a lower value.

5.1.6 The board also agrees with the appellant that D5 does not disclose starting a contention prevention period when the at least one component requests access to the data line. The decision states that the "remaining time" of the data transfer period after the last losing master has "left the bus" (the board understands this to mean "ceased transmitting") can be regarded as a contention prevention period and that the start condition can be regarded as a media access request. Even if, for the sake of argument, the start condition in D5 were to be understood as a "media access request", the "contention prevention period" in D5 would not follow the "media access request" and thus would not be a "contention prevention period" in the meaning of the claims.

5.1.7 The claimed "low power mode", which covers both the embodiments described of no clock and a reduced clock frequency, can be read onto two different aspects of the disclosure of D5. Firstly, the bus being free can be seen as the claimed "low power mode" in the sense of there being no clock, since both the clock and data lines remain HIGH. Secondly, the claimed "low power mode" can be understood as a lower clock frequency, which is what occurs during the arbitration period preceding an Hs-mode data transfer. On either

interpretation, in terms of claim 1 of the main request, D5 discloses a method for media access control by a media access controller connected to a data line and a clock line, the media access controller being adapted to monitor the data line. In terms of claim 12 of the main request, D5 also discloses a device comprising multiple components coupled to a data line and a clock line comprising a media access controller adapted to monitor the data line. Turning to the computer readable medium claim 21, in view of the reference in D5 to a microcontroller (see page 4, left column, line 8), D5 discloses a computer readable medium having stored thereon a set of instructions.

5.2 *Document D1*

5.2.1 D1 relates to reducing the power consumption of a system by using a "central arbiter" (see figure 1; 1) connected to a CPU by a system bus to turn off the clock to a group of sub-circuits (see figure 1; 11 to 14), also connected to the system bus, if none of the sub-circuits requires a clock; see abstract and column 1, line 61, to column 2, line 9. The arbiter circuit monitors the system bus and, upon detecting that the sub-circuits will require the clock signal, re-enables the clock signal to the sub-circuits.

5.2.2 The board agrees with appellant's assessment of the disclosure of D1 that the arbiter decides to supply the clock to the sub-circuits based on addresses and/or commands from the CPU and not based on requests from the sub-circuits. Moreover, as the arbiter does not control access to a bus, D1 does not disclose a media access controller or a media access request.

6. *Novelty in view of D5, Article 54(1,2) EPC 1973*

6.1 The subject-matter of both claims 1 and 21 according to the main request differs from the disclosure of D5 in the following features:

- a. generating at least one media access grant in response to at least one media access request,
- b. the media access controller monitoring the data line, while maintaining at least the clock line in a low power mode, to detect the media access request generated by at least one component coupled to the data line and to the clock line,
- c. the media access controller forcing the clock line to exit the low power mode and starting a contention prevention period, when at least one component requests to access the data line or when the media access controller determines to transmit information itself.

In addition the subject-matter of claim 21 differs from the disclosure of D5 in the following feature:

- d. the set of instructions being executable by a media access controller.

6.2 The subject-matter of claim 12 differs from the disclosure of D5 in corresponding device features, namely in the media access controller being adapted to:

- a. to generate at least one media access grant,
- b. to monitor the data line, while maintaining at least a clock line in a low power mode, to detect

at least one media access request for said data line generated by at least one of said components and

- c. to force the clock line to exit the low power mode and to start a contention prevention period, in response to at least one detected media access request or when the media access controller determines to transmit information itself.
- 6.2.1 Consequently the subject-matter set out in all three independent claims is new, Article 54(1,2) EPC 1973, in view of the disclosure of D5.
7. *Novelty in view of D1, Article 54(1,2) EPC 1973*
- 7.1 The subject-matter of all three independent claims differs from the disclosure of D1 at least in the features of media access control, generating a media access request and generating a media access grant.
- 7.2 Consequently the subject-matter set out in all three independent claims is also new, Article 54(1,2) EPC 1973, in view of the disclosure of D1.
8. *Remittal to the first instance, Article 111(1) EPC 1973*
- 8.1 Since the appealed decision was only based on lack of novelty, Article 54(1,2) EPC 1973, in view of D5 and the board finds that the application overcomes this objection, the case is remitted to the first instance for further prosecution on the basis of the main request in order that the examining division can *inter alia* also consider inventive step, Article 56 EPC 1973.

- 8.2 Thus the examining division will also have an opportunity to consider whether the following issues give rise to objection under the EPC:
- 8.2.1 Claim 1 of the main request refers to "**the** media access controller", "**the** data line" and "**the** clock line" (in each case emphasis by the board) without a respective antecedent. Also in claims 7 and 8 "pervious" should presumably read "previous". Hence claims 1, 7 and 8 may not comply with Article 84 EPC 1973 regarding clarity.
- 8.2.2 The expression "incorporated herein by reference" on page 1, line 23, and page 2, line 12, the expression "scope of the invention" on page 4, line 5, the expression "spirit of the invention" on page 21, lines 5 to 6, and the expressions "the spirit and the scope" and "the spirit and scope" on page 30, lines 16 and 19, respectively, may constitute unnecessary statements, Rule 34(1)(c) EPC 1973.

Order

For these reasons it is decided that:

The decision under appeal is set aside.

The case is remitted to the first instance for further prosecution on the basis of the main request.

The Registrar:

The Chairman:

A. Counillon

D. H. Rees