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**Datasheet for the decision  
of 20 March 2013**

**Case Number:** T 1512/09 - 3.5.06  
**Application Number:** 05006951.7  
**Publication Number:** 1582958  
**IPC:** G06F 1/00, G01R 31/3185,  
G06F 12/14  
**Language of the proceedings:** EN

**Title of invention:**

Method and system for protecting content in a programmable system

**Applicant:**

Emma Mixed Signal C.V.

**Headword:**

Content protection/EMMA MIXED SIGNAL

**Relevant legal provisions (EPC 1973):**

EPC Art. 56

**Keyword:**

"Inventive step - yes"

**Decisions cited:**

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**Catchword:**

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Case Number: T 1512/09 - 3.5.06

**DECISION**  
of the Technical Board of Appeal 3.5.06  
of 20 March 2013

**Appellant:** Emma Mixed Signal C.V.  
(Applicant) Naritaweg 165  
Telestone 8  
NL-1043 BW Amsterdam (NL)

**Representative:** Manitz, Finsterwald & Partner GbR  
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**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted 23 February 2009  
refusing European patent application  
No. 05006951.7 pursuant to Article 97(2) EPC.

**Composition of the Board:**

**Chairman:** D. H. Rees  
**Members:** G. Zucka  
M.-B. Tardo-Dino

## Summary of Facts and Submissions

I. The appeal is against the decision by the examining division, with reasons dispatched on 23 February 2009, to refuse European patent application 05006951.7, on the basis that the subject-matter of the independent claim 1 was not inventive, Article 56 EPC 1973. The following documents were cited during the first instance procedure:

D1: US 6 331 784 B1  
D2: US 2001/016 916 A1  
D3: US 4 698 750 A  
D4: US 2003/212 897 A1  
D5: WO 03/081 400 A

II. A notice of appeal was received on 30 April 2009, the appeal fee being paid on the same day. A statement of the grounds of the appeal was received on 6 July 2009.

III. The appellant requested that the decision be set aside and a patent granted on the basis of the main request that was the subject of the refusal or on the basis of the auxiliary request filed with the grounds of appeal.

IV. The documents of the main request are description pages 1 and 4 to 16 as originally filed and pages 2, 2a and 3 received on 19 April 2007, claims 1 to 25 as received on 19 April 2007, and drawing sheets 1 to 3 as originally filed.

The documents of the auxiliary request are claims 1 to 25 filed with the grounds of appeal and the same description and drawings as the main request.

V. The independent claim 1 of the main request reads as follows:

A method of protecting content embedded in a programmable system, the system having at least one Application Specific Integrated Circuit (ASIC) (12) executing an application,

characterized in that the system (10) comprises a non-volatile (NV) storage element (40) including a protected region (40A) and an unprotected region (40B) for storing information on the application, the ASIC (12) and the NV storage element (40) being encapsulated inside the system (10),

the method comprising the steps of:

(1) assigning at least one of a plurality of access modes to at least one access port (50, 50A, 50B), the access modes including at least an unrestricted access mode and a restricted access mode;

(2) in the unrestricted access mode, accepting one or more access port commands provided by an external device (2) through the access port (50, 50A, 50B), including the step of:

in response to an access port command, allowing a content stored in the system (10) to be visible to the external device (2) via the access port, including allowing visibility to a content of the protected region (40A) and a content of the unprotected region (40B);

(3) in the restricted access mode, accepting a limited set of access port commands provided by the external device (2) through the access port (50, 50A, 50B), including the step of:

in response to an access port command, restricting visibility of the content stored in the system (10), including allowing visibility to the content of the unprotected region (40B) and rejecting visibility to the content of the protected region (40A),

(4) switching the restricted access mode to the unrestricted access mode without exposing at least the content of the protected region (40A) to the external device (2) via the access port (50, 50A, 50B).

The independent claim 12 of the main request is an apparatus claim with apparatus features that correspond to the method features of claim 1.

- VI. The difference between the independent claim 1 of the auxiliary request 1 and that of the main request can be summarised in that the NV memory is accessed through the access port using the ASIC and the ASIC controls the restriction of the visibility of the different memory regions in different access modes. The independent Claim 12 of the auxiliary request contains similar changes.

### **Reasons for the decision**

1. Reference is made to the transitional provisions in Article 1 of the Decision of the Administrative Council of 28 June 2001 on the transitional provisions under Article 7 of the Act revising the European Patent Convention of 29 November 2000, for the amended and new provisions of the EPC, from which it may be derived which Articles of the EPC 1973 are still applicable to

the present application and which Articles of the EPC 2000 shall apply.

2. *The admissibility of the appeal*

In view of the facts set out at points I and II above, the appeal is admissible, since it complies with the EPC formal admissibility requirements.

3. *The procedural steps*

Pursuant to Article 12(3) RPBA, the board may decide the case at any time after filing of the statement of grounds of appeal. In the present case, given that the appellant's main request, with the application documents currently on file, is considered to be allowable as it stands (see below), the board judges it appropriate to issue a decision without issuing a prior notification or holding oral proceedings.

4. *Main request*

4.1 *Interpretation of the term "Application Specific Integrated Circuit (ASIC)"*

The board considers that for the skilled person both the term "Application Specific Integrated Circuit" and its acronym ASIC have a well-defined meaning. Notably, a "Field-Programmable Gate Array" (FPGA) is not an ASIC, although they may both be forms of gate array, since ASICs do not have re-configurable logic. As illustration, the entry "gate array" (redirected from the entry "ASIC") in the Microsoft Computer Dictionary, Fifth Edition, reads as follows:

**gate array** *n.* A special type of chip that starts out as a nonspecific collection of logic gates. Late in the manufacturing process, a layer is added to connect the gates for a specific function. By changing the pattern of connections, the manufacturer can make the chip suitable for many needs. This process is very popular because it saves both design and manufacturing time. The drawback is that much of the chip goes unused. *Also called:* application-specific integrated circuit, logic array.

The aspect of this definition which is most relevant for the inventive step assessment given below is that the gates are connected for a specific function. In other words, the connections are "hard-wired", *i.e.* an ASIC is not a *programmable* logic chip as disclosed in D1. Thus the board does not agree with the position taken in the appealed decision that the FPGA of D1 is an ASIC as claimed. On the other hand the board considers it well known that an FPGA, together with the necessary configuration memory to program the logic of the FPGA, is a common alternative to an ASIC. Which is used in a particular application depends on a variety of factors, for example the production volume; ASICs are cheap in very large quantities but very expensive in small quantities.

#### 4.2 *Inventive step, Article 56 EPC 1973*

The closest prior art was argued by the examining division to be document D1. This view is not actually disputed by the appellant, although the appellant does contest (in the grounds of appeal, pages 2 to 6) the

first instance's assessment with regard to the disclosure of some of the elements of claim 1 by D1. In this context the board notes that D1 does not indicate what function the FPGA, once configured, carries out. Thus it does not disclose that the FPGA "execut[es] an application". Further, while it may be a matter of common knowledge that it is possible to implement a programmable processor in an FPGA, that is not itself part of the disclosure of D1. Otherwise, since it has no effect on the outcome of the proceedings, the board assumes for the sake of argument that the assessment in the appealed decision regarding which elements of claim 1 are disclosed by D1 is essentially correct. It is therefore assumed for the sake of argument that D1 discloses:

A method of protecting content embedded in a system, the system having a programmable logic chip,

the system comprising a non-volatile (NV) storage element, the programmable logic chip and the NV storage element being encapsulated inside the system,

the method comprising the steps of:

(1) assigning one of a plurality of access modes to an access port, the access modes including an unrestricted access mode and a restricted access mode;

(2) in the unrestricted access mode, accepting access port commands provided by an external device through the access port, including the step of in response to an access port command, allowing a content stored in the system to be visible to the external device via the access port;

(3) in the restricted access mode, accepting a limited set of access port commands provided by the external device through the access port, including the



step of in response to an access port command, restricting visibility of the content stored in the system,

(4) switching the restricted access mode to the unrestricted access mode without exposing protected content to the external device via the access port.

The subject-matter of claim 1 therefore differs at least from the method disclosed by D1 in that (1) an ASIC, rather than an FPGA, (2) executes an application, (3) information "on" (*i.e.* concerning) the application is stored in non-volatile storage and (4) the non-volatile storage is divided into a region where the protection is applied and an unprotected region that can be accessed in all access modes.

Regarding feature (1), which solves the objective problem of providing a protection against reverse engineering, the board notes that the whole point of the method disclosed in D1 is to protect the configuration memory of an FPGA from unauthorised copying (see D1, column 1, lines 9 to 11). In fact, the schemes disclosed in D1 are introduced to deal with a transition *from* ASICs to programmable logic circuitry (see column 1, lines 14 to 20) and it is not apparent from D1 or otherwise why the skilled person would want to transition *back* to an ASIC whilst still applying a scheme as disclosed in D1. Indeed, whereas FPGAs have such a memory, from which they load their configuration when powered up, ASICs are permanently configured through hard-wiring and have no need for a similar configuration memory that would have to be protected against the same kind of design theft (see D1, column 1, lines 17 to 25).

The appealed decision points out (Reasons 4) that "Furthermore, the present application does not draw a clear distinction between FPGA and ASIC. The feature of reprogramming the device defined by claim 1 points more to FPGA rather than to ASIC, from which the skilled person would expect the logic being "hard-wired" into the chip. The application does not provide a delimiting feature by which the use of an ASIC would show an advantage or a different technical effect over the use of an FPGA". This wording seems to imply that claim 1 would have been drafted keeping in mind at least the possibility of using an FPGA instead of an ASIC, *i.e.* its subject-matter would really not be that far away from a method that employs an FPGA, as in D1. However, according to the board, an ASIC is clearly a different thing than an FPGA (see 4.1 above) and claim 1 clearly and explicitly refers to an ASIC, not to an FPGA or some other programmable circuitry. Even if the claim also refers to a "programmable system", the claim's wording leaves no doubt that, in that system, it is not the logic of the ASIC which is programmable in the sense of "re-configurable". In fact, the logic of an ASIC itself can not be programmed, by its very nature. Thus the claim cannot be construed in this way. Rather, as is confirmed by the description of the present application (page 5, lines 17 to 23), the intention is for the ASIC to be programmable in the sense of carrying out a computer program, in the form of algorithms in the non-volatile memory. The ASIC of claim 1 is therefore clearly distinct from the FPGA of D1.

Thus evidently the claimed subject-matter is not obvious starting from D1. The examining division did not at any point put forward any of the other cited documents as a suitable starting point (only D4 was cited for one feature that the examining division considered distinguishing), and the board concurs. The board therefore concludes that the subject-matter of claim 1 of the main request satisfies the requirement of Article 56 EPC 1973.

For similar reasons, the subject-matter of the corresponding system claim 12, as well as the subject-matter of the dependent claims 2 to 11 and 13 to 25 also satisfies the requirement of Article 56 EPC 1973.

- 4.3 There are no other objections raised by the examining division which are still outstanding, nor are any apparent to the board. The main request is therefore allowable.
  
5. Given that the main request is allowable, there is no need to comment the auxiliary request.

**Order**

**For these reasons it is decided that:**

1. The appealed decision is set aside.
  
2. The case is remitted to the department of first instance, with the order to grant a patent on the basis of the current main request.

The Registrar:

The Chairman:

B. Atienza Vivancos

D. H. Rees