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**Datasheet for the decision
of 10 August 2011**

Case Number: T 1467/09 - 3.5.03

Application Number: 06025990.0

Publication Number: 1933221

IPC: G05F 1/56

Language of the proceedings: EN

Title of invention:

Voltage regulator with an improved transient response

Applicant:

Infineon Technologies AG

Headword:

Voltage regulator/INFINEON

Relevant legal provisions:

EPC Art. 56

Relevant legal provisions (EPC 1973):

-

Keyword:

"Inventive step (yes)"

Decisions cited:

-

Catchword:

-



Case Number: T 1467/09 - 3.5.03

D E C I S I O N
of the Technical Board of Appeal 3.5.03
of 10 August 2011

Appellant: Infineon Technologies AG
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Decision under appeal: Decision of the examining division of the
European Patent Office posted 12 January 2009
refusing European patent application
No. 06025990.0 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: A. S. Clelland
Members: F. van der Voort
M.-B. Tardo-Dino

Summary of Facts and Submissions

- I. This appeal is against the decision of the examining division refusing European patent application No. 06025990.0 (publication number EP 1 933 221 A).
- II. The reasons given for the refusal were that the claimed subject-matter did not involve an inventive step having regard to the disclosure of

D1: US 2004/0239304 A1

and taking into account the common general knowledge of a person skilled in the art (Article 56 EPC) and that the independent claims were not in the two-part form in accordance with Rule 43(1) EPC.

- III. In addition to D1 cited above, the following documents were cited in the European search report:

D2: US 6 744 288 B;

D3: "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator", G. A. Rincon-Mora *et al*, IEEE Journal of Solid-State Circuits, Vol. 33, No. 1, January 1998, pages 36 to 44; and

D4: US 2002/0185681 A.

Apart from D1, in the course of the examination procedure reference was made to D2 and D3 (the board notes that in the decision under appeal at point I.3 the numbers "D2" and "D3" were erroneously interchanged).

IV. In the notice of appeal the appellant requests that a patent be granted on the basis of claims 1 to 9 as filed during the oral proceedings before the examining division and on which the decision under appeal is based. In the statement of grounds of appeal the appellant gave arguments in support of its request and conditionally requested oral proceedings.

V. Claims 1 to 9 consist of independent claims 1 and 6 and dependent claims 2 to 5 and 7 to 9.

Independent claim 1 reads as follows:

"A voltage regulator comprising

- a power field effect transistor (M_p) having a threshold voltage (V_{th}), a drain terminal receiving an input voltage (V_{in}), a source terminal providing an output voltage (V_{out}) and a load current (I_{load}), a gate terminal responsive to a control signal (V_g), and a bulk terminal,
- a control-loop circuit (10) responsive to said output voltage (V_{out}) and providing said control signal (V_g), said control circuit being adapted for adjusting said control (V_g) signal to such a value that said output voltage (V_{out}) is regulated to a constant value, and
- a switching circuit (20) responsive to said output voltage (V_{out}) and/or to said load current (I_{load}), said switching circuit being adapted for connecting said bulk terminal (B) either with said source terminal (S) or with a constant potential (V_2) lower than a source potential (V_{out}) of the transistor dependent on said load current and/or

said output voltage (V_{out}), such that said threshold voltage (V_{th}) of said power field effect transistor (M_p) is modified dependent on said load current (I_{load}) and/or said output voltage (V_{out})."

Independent claim 6 reads as follows:

"A method for controlling a power field effect transistor (M_p) having a threshold voltage (V_{th}), a drain terminal receiving an input voltage (V_{in}), a source terminal providing an output voltage (V_{out}) and a load current (I_{load}), a gate terminal responsive to a control signal (V_g), and a bulk terminal; said method for regulating the output voltage to a desired constant value comprising:

- modifying said threshold voltage dependent on said load current (I_{load}) and/or said output voltage (V_{out}), by connecting said bulk terminal either with said source terminal or with a constant potential (V_2) lower than a source potential (V_{out}) of the transistor (M_p) dependent on said load current (I_{load}) and/or said output voltage (V_{out})."

Reasons for the Decision

1. *Inventive step*

- 1.1 Both the examining division and the appellant consider D1 and, more specifically, the circuit diagram of Fig. 6, as representing the closest prior art.

1.2 D1 (Fig. 6) discloses, using the language of claim 1, a voltage regulator 600 which includes:

- an NMOS field effect transistor 618 having a threshold voltage V_t (paragraphs [0001] and [0009]), a drain terminal receiving an input voltage V_{IN_PWR} , a source terminal providing an output voltage V_{REG} and a load current I_L , a gate terminal responsive to a control signal (at line 614), and a back gate;
- a control-loop circuit 602-612 responsive to the output voltage V_{REG} and providing the control signal at line 614, the control-loop circuit being adapted to adjust the control signal to such a value that the output voltage V_{REG} is regulated to a desired, i.e. constant, value (as determined by voltage reference 602); and
- a back gate potential control circuit including a sense transistor 616, a current mirror including transistors 644, 648, and a diode 628 connected in parallel to a voltage divider defined by resistors 622 and 624 (with values R_A and R_B , respectively), in which the back gate potential control circuit is responsive to the output voltage V_{REG} and/or to the load current I_L and is adapted to connect the back gate of NMOS field effect transistor 618 either with its source terminal or with a second potential, dependent on the load current and/or the output voltage V_{REG} , such that the threshold voltage V_t of the field effect transistor 618 is modified dependent on the load current I_L and/or the output voltage V_{REG} .

More specifically, if the load current I_L is zero, i.e. V_{REG} is zero, the current sensed by transistor 616 and

the mirrored current through line 640 are zero and, hence, the voltage drop over resistor 624 is zero and the back gate potential of transistor 618 is equal to its source potential, whereas if there is a load current flowing through the load 636 the back gate potential is increased to a second potential equal to $V_{REG} + V_{BE} \cdot R_B / (R_A + R_B)$, in which V_{BE} is the forward voltage of diode 628. Due to this potential increase, a forward bias is applied to the source/back gate junction of transistor 618, thereby reducing the threshold voltage V_t of the transistor (paragraph [0032]). The back gate potential control thereby allows the voltage regulator of Fig. 6 to have a very low leakage current at essentially zero load current and a reduced input voltage for generating the same non-zero output voltage at higher load currents (page 3, left-hand column, lines 1 to 10, and right-hand column, lines 2 to 11, and paragraph [0032]).

- 1.3 The board notes that in the art of MOS field effect transistors the term "back gate" as used in D1 is synonymous with "bulk terminal" as used in claim 1.
- 1.4 The subject-matter of claim 1 differs from the voltage regulator disclosed in D1 at least in that according to claim 1 the above-mentioned second potential at the back gate, i.e. bulk terminal, is lower than the source potential of the field effect transistor.
- 1.5 Since according to claim 1 the source terminal provides the output voltage, i.e. the power field effect transistor is in a common drain topology, the "input voltage" at the drain terminal is understood as the unregulated voltage which, in terms of its absolute

value, must be higher than the regulated output voltage. Similarly, the feature that the above-mentioned second potential is lower than the source potential is understood as relating to the absolute values of these potentials.

The technical effect of changing the back gate potential to a second potential which is lower than the source potential in this topology is that the threshold voltage of the field effect transistor is thereby increased (cf. the application as published, column 4, lines 38 to 43). Due to the feedback provided by the control-loop circuit this in turn results in a higher voltage, i.e. an extra charge, at the gate in order to maintain the output voltage at the same constant value (application as published, col. 6, lines 2 to 5).

This extra charge may be used in order to improve the control speed of the control-loop circuit and, hence, the overall performance of the voltage regulator, by using it as a precharge for switching-on the field effect transistor in response to an increase in the load current and at the same time decreasing the threshold voltage back to its previous, higher value (application as published, paragraph [0024]).

- 1.6 As to the above-mentioned distinguishing feature (which the examining division held to be the only distinguishing feature), the examining division argued as follows (see the decision under appeal, point II.9.1):

"The problem to be solved by the present invention may therefore be regarded as merely adapting the

circuit to a power field effect transistor with different properties.

The feature of connecting the bulk terminal either to the source terminal or to a constant voltage being lower than the source voltage, instead of either to a constant voltage being higher than a source voltage or to the source terminal as shown in D1, *de facto* only shifts the two voltages applied to the bulk terminal of [sic] a predetermined amount. This is a slight modification which is matter of normal design procedure for the person skilled in the art faced to [sic] the above-mentioned problem.

Therefore, the subject-matter of claim 1 does not involve an inventive step in the sense of Article 56 EPC."

- 1.7 The board does not find this reasoning convincing for the following reasons:

As regards the formulation of the technical problem, it is unclear what is meant by "different properties". The board notes, for example, that the field effect transistor 618 referred to in D1 (Fig. 6) is of n-type and that the field effect transistor as specified in claim 1 may also be of n-type and, hence, would at least in this respect have the same properties.

Further, whilst it is true that, on comparing the claimed voltage regulator and the voltage regulator of Fig. 6 of D1, the voltages which are respectively applied to the bulk terminal are *de facto* shifted by a

certain amount, it is unclear why this would constitute only a slight modification of the known regulator and why this would be a matter of normal design procedure for the person skilled in the art when faced with the above-mentioned problem. For example, if the second bulk terminal potential of transistor 618 in Fig. 6 were made lower than the source potential, the technical effect would be an increase in the threshold voltage rather than the desired reduction in the threshold voltage. Hence, this would clearly go against the teaching of D1, cf. point 1.2 above.

Further, if the voltage regulator of Fig. 6 of D1 were to be made suitable for use with a p-type field effect transistor, the skilled person would find a solution in D1, Fig. 3, which discloses a voltage regulator which includes a field effect transistor 318 of p-type in a common source topology. As follows from Fig. 3, the back gate potential is set equal to either the source potential or a second potential which is lower than the source potential, see also paragraph [0022] and equation (3). However, the effect of applying the second potential at the back gate would remain the same as in Fig. 6, i.e. the threshold voltage would thereby be reduced (D1, page 3, left-hand column, lines 4 to 8 and 29 to 33). This is contrary to the technical effect of increasing the threshold voltage as achieved by the claimed regulator (see point 1.5 above).

The board therefore concludes that D1 neither discloses nor suggests a voltage regulator as claimed in claim 1.

1.8 In the board's view, at the filing date of the application in suit it was part of the common general

knowledge of a person skilled in the art that the threshold voltage of a MOSFET is a function of the back gate (or bulk) potential. This functional relationship is known as the body effect, the substrate (bias) effect, or the back gate effect and in D4 use is made of this effect in order to reduce leakage currents.

More specifically, D4 discloses two circuits (Figs 9 and 10) in which a reverse bias voltage is applied to the bulk, i.e. the substrate. In the circuit of Fig. 9 of D4 a power NMOS transistor Tr1 has its source terminal connected to ground potential and its drain terminal connected via a load 44 to a high potential of a power source (page 5, paragraph [0067]). When the transistor is set in the ON state, the substrate potential is set to 0 V, i.e. the source potential, and, when it is set in the OFF state, a voltage $-V_g$, e.g. -5 V, is applied to the substrate by way of a substrate reverse bias potential. Thereby, the level of charging current which flows in a stray gate-substrate capacity is made extremely small (paragraph [0068]). Fig. 10 of D4 shows a circuit which is similar to the circuit of Fig. 9 and in which, by applying a reverse bias to the substrate in the OFF state, the threshold voltage V_t of the transistor Tr1 is increased (paragraph [0073]).

It is noted that both circuits are driver circuits for switching ON/OFF a load 44 rather than voltage regulator circuits. Further, the power NMOS transistor Tr1 is in a common source topology. Nevertheless, for the sake of argument, if a person skilled in the art were to apply for the same purpose, i.e. reducing the leakage current in the transistor's OFF state, the

teaching of D4 to the voltage regulator of D1, it is arguable that he/she would provide, in accordance with the teaching of D4, a control means for applying a constant reverse bias potential to the back gate of the transistor 618 of Fig. 6 of D1 when the transistor is in the OFF state. However, the back gate potential for the ON state would not require any modification and, hence, would still be determined by the voltage divider defined by the resistors 622 and 624. This implies that the back gate, i.e. the bulk terminal, would at no instance be connected to the source terminal of the transistor 618, whereas the voltage regulator of claim 1 requires that the switching circuit be adapted to connect the bulk terminal either with the source terminal or with a constant potential lower than a source potential of the transistor dependent on the load current and/or the output voltage.

Hence, starting out from D1 and taking into account the common general knowledge and/or the teaching of D4, the skilled person would not have arrived at a voltage regulator which includes all the features of claim 1 without exercising inventive skill.

- 1.9 The same conclusion is arrived at if D3, which, like D1 and the present invention, relates to a voltage regulator, were taken as representing the closest prior art, since the voltage regulator disclosed in D3 operates in the same way as the voltage regulator disclosed in D1. More specifically, Fig. 6 of D3 illustrates a voltage regulator in which a Schottky diode is used for forward biasing the source/bulk junction of a PMOS pass device (M_{po}) in a common source topology. This results, as in D1, in a reduction of the

threshold voltage (page 39, section III.B, lines 1 to 11). The board notes that the regulator of D3, Fig. 6, is essentially the same as the regulator shown in D1, Fig. 2 (Schottky diode 239).

1.10 Further, as to the remaining prior art document on file, i.e. D2, the board notes that D2 discloses a digital output driver stage 100 (D2, Fig. 1) which includes a PMOS power transistor M0. The voltage on the n-bulk of the transistor M0 is pulled down to ground when the transistor is turned on and is pulled up to supply voltage (which is equal to the source voltage, see Fig. 1) when the transistor is turned off. This bulk potential control essentially corresponds to what is described in D1 in respect of the control of PMOS pass transistor 318 of Fig. 3 and the same advantages are achieved, i.e. a low leakage current and a lower threshold voltage enabling an operation at a lower supply voltage, thereby requiring less power to operate, cf. D2, col. 5, lines 24 to 36, and D1, page 3, left-hand column, lines 4 to 10 and page 3, right-hand column, lines 2 to 11.

1.11 The board thus concludes that, taking into account the common general knowledge of a person skilled in the art, none of the prior art documents on file or any combination thereof discloses or suggests a voltage regulator including all the features of claim 1. The subject-matter of claim 1 therefore involves an inventive step having regard to the disclosure of the prior art documents on file and the common general knowledge of the person skilled in the art (Articles 52(1) and 56 EPC).

1.12 The above reasons apply, *mutatis mutandis*, to independent method claim 6, it being noted that, since the method is for regulating the output voltage to a desired constant value, the same technical effect as referred to at point 1.5 above is achieved. Further, since claims 2 to 5 and 7 to 9 are dependent claims, the subject-matter of these claims also involves an inventive step.

2. *Rule 43(1) EPC*

2.1 The board notes that according to the minutes of the oral proceedings before the examining division the chairman pointed out that claim 1 did not comply with Rule 43(1)(b) EPC (see the minutes, point 2). Further, according to these minutes, the application was refused because it did not meet the requirements of Article 56 EPC (the minutes, point 6 and "Sheet 2/1", lines 2 to 4). In the written decision, however, the application is refused on both grounds, see the decision under appeal, points 9 to 11. More specifically, it was held that claims 1 and 6 "are not in the two-part form in accordance with Rule 43(1) EPC, which in the present case would be appropriate".

Apart from this inconsistency between the minutes and the written decision which causes some uncertainty as to what the examining division actually intended to decide, the board notes that neither in the minutes nor in the written decision any reasons were given as to why in the present case it would have been appropriate to cast the independent claims in the two-part form.

2.2 In the board's view, in the present case, the relevant prior art is fairly acknowledged in the application documents on file. In particular, Fig. 1 illustrates a conventional voltage regulator and the amended description page 2, as filed with the letter of 29 May 2007, explicitly acknowledges that D1 discloses a voltage regulator in which the back gate of the pass transistor is biased with respect to the source by a fractional part of the forward voltage of a diode. From this it is clear that, contrary to the claimed subject-matter, the back gate bias potential is set higher than the source potential. In the present case, the board does not therefore see a reason to insist on a two-part form of the independent claims.

3. For the above reasons, the decision under appeal is to be set aside.

4. The board further notes that the claims on file have not been amended in such a way that they contain subject-matter which extends beyond the content of the application as filed. More specifically, claim 1 is based on claims 1, 2, 6 and 8 as filed and the description, col. 4, lines 27 to 43 (reference is made to the application as published). Claims 2 to 4 correspond to claims 3 to 5 as filed and claim 5 is based on claim 7 as filed and col. 4, lines 34 to 36. Claim 6 is based on claims 1, 6, 8 and 9 as filed and the description, col. 4, lines 27 to 43. Claims 7 to 9 correspond to claims 10 to 11 as filed.

The board is therefore satisfied that the amendments do not give rise to objections under Article 123(2) EPC.

Neither do the claims in the board's view give rise to objections under Article 84 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the department of first instance with the order to grant a patent on the basis of the following documents:
 - claims 1 to 9 as filed during the oral proceedings before the examining division;
 - amended pages 2, 2a and 3 of the description as filed with the letter of 29 May 2007, together with pages 1 and 4 to 9 as originally filed; and
 - drawing sheets 1/4 to 4/4 as originally filed.

The Registrar:

The Chairman:

G. Rauh

A. S. Clelland