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# Datasheet for the decision of 14 March 2013

**Case Number:** T 1029/09 - 3.5.04

**Application Number:** 03754870.8

**Publication Number:** 1554732

**IPC:** G11C7/06, G11C7/10

**Language of the proceedings:** EN

**Title of invention:**
HIGHLY COMPACT NON-VOLATILE MEMORY AND METHOD THEREOF

**Applicant:**
SanDisk Technologies Inc.

**Headword:**

**Relevant legal provisions:**
EPC 1973 Art. 56

**Keyword:**
Inventive step - after amendment

**Decisions cited:**

**Catchword:**

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**Beschwerdekammern**
**Boards of Appeal**
**Chambres de recours**

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

**Case Number: T 1029/09 - 3.5.04**

# D E C I S I O N
# of Technical Board of Appeal 3.5.04
# of 14 March 2013

| | |
|---|---|
| **Appellant:** (Applicant) | SanDisk Technologies Inc.<br>Two Legacy Town Center<br>6900 North Dallas Parkway<br>Plano, Texas 75024 (US) |
| **Representative:** | Hitchcock, Esmond Antony<br>Marks & Clerk LLP<br>90 Long Acre<br>London<br>WC2E 9RA (GB) |
| **Decision under appeal:** | **Decision of the Examining Division of the European Patent Office posted on 26 November 2008 refusing European patent application No. 03754870.8 pursuant to Article 97(2) EPC.** |

**Composition of the Board:**

**Chairman:** F. Edlinger
**Members:** R. Gerdes
B. Müller

## Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 03 754 870.8.

II. In the decision under appeal the examining division held that the application did not comply with Article 56 EPC because the subject-matter of claims 1 and 21 according to the applicant's sole request did not involve an inventive step in view of:

D1: US 5 940 329 A.

III. The appellant appealed against this decision and with the statement setting out the grounds of appeal filed an amended set of claims. In a communication annexed to the summons to oral proceedings, the board *inter alia* indicated that it tended to share the appellant's opinion that

D3: US 6 396 736 B1

constituted the closest prior art with respect to the subject-matter of the amended claims.

IV. Oral proceedings were held on 14 March 2013. The appellant withdrew the previous requests on file and submitted new claims 1 to 15 entitled "Main Request" as the final sole request. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims submitted in the oral proceedings and a description to be adapted.

V. The independent claims read as follows:

"1. A non-volatile memory device, comprising an array of multi-state memory cells (300) addressable by a plurality of word lines and bit lines, a bank of read/write circuits arranged to operate on a group of memory cells in parallel via an associated group of bit lines, the memory cells of the group of memory cells connected by a word line of the plurality of word lines, with each read/write circuit being partitioned into a core portion (210) and a common portion (22);

CHARACTERISED BY:

the bank of read/write circuits (370) being organized into multiple subgroups thereof, with each subgroup forming a stack (400) of read/write circuits comprising multiple core portions (410) from individual read/write circuits of the subgroup, each of the multiple core portions (410) coupleable to a bit line of the bit lines for simultaneous read or programming access by the multiple core portions (410) in a stack;

wherein each core portion has a width extending in a direction orthogonal to a direction in which the bit lines extend and comprises a sense amplifier (212) arranged to sense a conduction current level of an addressed memory cell, wherein a number of core portions in each subgroup is the same as a number of bit lines the multiple core portions are arranged to couple to for simultaneous read or programming access and over which the width of each of the core portions extends;

wherein each stack further comprises a common portion (420) including a processor (222) coupled to each of the multiple core portions (410) of the subgroup and arranged to process data associated with the multiple

core portions of the subgroup, and wherein the core portions and the common portion are stacked in the direction in which the bit lines extend; and

wherein the processor (222) in each common portion is coupled to receive the conduction current level sensed from the sense amplifiers (212) of the respective stack and arranged to compute a set of data bits from the conduction current level sensed;

each subgroup including a bus (431) interconnecting each core portion of the subgroup and the common portion among the stack, enabling serial communication between the each core portion and the common portion."

and

"15. A method of forming a compact group of read/write circuits for a non-volatile memory device, comprising:

providing the bank of read/write circuits for operating on a group of multi-state memory cells (300) in parallel via an associated group of bit lines (211), the memory cells of the group of memory cells connected by a word line;

partitioning each read/write circuit into a core portion (210) and a common portion (220), wherein each core portion comprises a sense amplifier (212) coupled via a bit line (211) among the associated group of bit lines, said sense amplifier (212) arranged to sense a conduction current level of an addressed memory cell;

CHARACTERISED BY:

organizing said bank of read/write circuits into multiple subgroups thereof, with each subgroup forming a stack of read/write circuits (370) having multiple core portions from individual read/write circuits of the subgroup, wherein each core portion has a width extending in a direction orthogonal to a direction in which the bit lines extend and wherein a number of core portions in each subgroup is the same as a number of bit lines the multiple core portions are coupled to and over which the width of each of the core portions extends;

wherein each stack further comprises a common portion coupled to each of the multiple core portions, wherein the core portions and the common portion are stacked in the direction in which the bit lines extend;

wherein each subgroup including a bus (431) interconnecting each core portion of the subgroup and the common portion among the stack, enabling serial communication between the each core portion and the common portion;

providing a processor (222) in the common portion (220) to process data associated with the multiple core portions of the subgroup; and

wherein the processor (222) in each common portion is coupled to receive the conduction current level sensed from the sense amplifiers (212) of the respective stack and computes a set of data bits from the conduction current level sensed."

Claims 2 to 14 depend on claim 1.

VI. In the decision under appeal the examining division considered that claim 1, when read onto D1, was only distinguished by the terms non-volatile and processor. The term processor could refer to any kind of data processing and the fact that claim 1 related to a non-volatile memory device did not justify an inventive step because this feature did not have "any technical interrelationship with the remaining features". The independent claims neither contained features relating to details of the bit line sensing circuits nor to current sensing (see points 2 and 3 of the reasons).

VII. The appellant's arguments may be summarised as follows:

The claims have been amended to unambiguously relate to a multi-state non-volatile memory device with conduction current sensing and subsequent processing to determine the storage state of the multi-state memory cells. D1 fails to disclose storing more than one bit of data in each of the memory cells. Moreover, D1 relates to DRAM technology, which relies on voltage sensing. The sensing technique of D1 therefore differs significantly from that of the present invention.

The independent claims have been formulated in the two-part form to indicate those features that characterise the invention over D3, which constitutes the closest prior art. D3 provides a single processor for interpreting the sensing results obtained from all of the memory cells arranged in parallel along a word line. D3 therefore fails to subdivide the group of memory cells connected to a word line into a number of subgroups such that a processor is allocated to each subgroup.

In addition, the subject-matter of claim 1 is distinguished from D3 by arranging each subgroup of read/write circuits consisting of multiple core portions and a shared common portion in a stack. D3 also does not disclose the serial bus interconnecting the core portions of each subgroup with the associated processor in the common portion. The objective technical problem is to increase operating speed whilst keeping a penalty incurred in terms of die space used for this purpose to a minimum. The solution to this problem as claimed provides a configuration in which the distance between the core and common portions can be minimised.

## Reasons for the Decision

1. The appeal is admissible.

2. Compared to the claims underlying the decision under appeal, the present set of claims has been restricted to a multi-state non-volatile memory device and a method of forming a compact group of read/write circuits for a multi-state non-volatile memory device, respectively. The core portions have been specified to each comprise a sense amplifier for conduction current sensing. Further limitations relate to the functionality provided by the processor in each common portion which computes a set of data bits from the sensed current levels. In addition, the present claims express in more detail the concept of a stack containing core portions and a common portion and being "stacked in a direction in which the bit lines extend". Further features have been added relating to the serial bus interconnecting the core portions and the common portion in each subgroup.

*3. Amendments (Article 123(2) EPC)*

3.1 The present independent claims are based on claims 1 and 30 as filed, respectively. The features relating to the multi-state memory cells, the sense amplifiers for conduction current sensing and the processing in each common portion to compute a set of data bits from the sensed conduction current level are disclosed in claims 5, 9 and paragraph [0109] of the application as filed. The features relating to the stacking of core and common portions are derivable from paragraphs [0089] and [0094], together with figure 10. Claims 2 and 3 of the original application disclose the serial interconnection of core and common portions.

3.2 Corresponding amendments have been made to independent claim 15. Hence, the board finds that the claims of the appellant's sole request do not contain subject-matter which extends beyond the content of the application as filed and thus comply with Article 123(2) EPC.

*4. Inventive Step (Article 56 EPC 1973)*

4.1 D1 was cited in the decision under appeal as being the closest prior art with respect to the subject-matter then claimed. D1 relates to a DRAM having an array of memory cells that are each capable of storing a single bit. The state of the cells is read in a single read operation by sensing a voltage change on a bitline (see abstract and column 1, lines 10 to 34 and column 2, lines 6 to 22). The amended independent claims unambiguously relate to multi-state non-volatile memory devices with conduction current sensing. As will be shown below, the board considers, in agreement with the appellant, D3 as the closest prior art on file.

4.2 D3 discloses a non-volatile memory device (see for example the abstract and figures 28 and 29) comprising an array of multi-state memory cells (3) that can be addressed by a plurality of word lines (6) and bit lines (5). D3 also shows a bank of read/write circuits (4, 21, 27) arranged to operate on a group of memory cells in parallel via an associated group of bit lines. In a read operation the conduction currents of a plurality of memory cells connected by a word line are sensed by a circuit consisting of a plurality of sense latches (4). For four-state memory cells three read operations are carried out. The three data bits resulting from the read operation of a single memory cell are processed in a CPU (27) to recover two data bits indicative of the state of the memory cell (see column 18, line 16 to column 20, line 9 and column 21, line 51 to column 23, line 20). Hence, D3 discloses a partitioning of the bank of read/write circuits into a core portion and a common portion, the core portion containing multiple sense latches coupling to the bit lines of the memory array for simultaneous read or programming access. The common portion comprises a processor (27) computing a set of data bits from the sensed conduction current levels.

4.3 D3 does not disclose the organisation of the bank of read/write circuits in multiple subgroups, each subgroup having multiple core portions and a common portion which is connected to the core portions of that subgroup via a serial bus. In D3 there is also no indication that the read/write circuits including the core portions and the common portion are arranged as a stack "in the direction in which the bit lines extend".

4.4 These distinguishing features of claim 1 allow to speed up the required logic operations which are necessary for read and write operations of the multi-state memory cells. In addition, the arrangement of core and common portions in each one stack for each subgroup of read/write circuits together with the provision of a serial bus interconnecting its components allows to minimise the wiring in a subgroup.

4.5 The board, therefore, essentially agrees with the appellant and considers the technical problem as how to increase the processing speed of the bank of read/write circuits and at the same time to provide an arrangement of read/write circuits such that the penalty incurred in terms of wiring complexity and die space can be minimised.

4.6 The present application refers to a "read/write stack ... implemented conventionally". The read/write modules in this stack each comprise one sense amplifier and one bit conversion logic, wherein the bit conversion logic can be considered as a processor in the sense of claim 1. The conventional implementation therefore provides one processing element per read/write/circuit operating in parallel and thus allows to increase the processing speed. It also discloses that "a read/write stack ... with a stack of eight read/write modules can be used to service eight columns in parallel" (see figures 6A and 6B as well as paragraphs [0032], [0035] and [0036]). However, the conventional implementation does not provide a common portion including a processor for a subgroup of read/write circuits comprising multiple core portions. It also does not show the interconnection of the common portion with each core portion via a serial bus so that the processor in the common portion is coupled to

receive the conduction current level sensed from the sense amplifiers of this subgroup. Therefore, the combination of the teaching of D3 with elements of the conventional implementation of the read/write modules as shown in figure 6 of the present application would not have resulted in a straightforward manner in the claimed subject-matter.

4.7 None of the other documents on file provides a hint at the solution to the above technical problem. As a consequence, the subject-matter of claim 1 involves an inventive step in view of the prior art on file (Article 56 EPC 1973).

4.8 The above reasoning applies likewise to independent claim 15 which is directed to a method of forming a compact group of read/write circuits for a non-volatile memory device corresponding to the device of claim 1. Claims 2 to 14 directly or indirectly depend on claim 1.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent with claims 1 to 15 submitted in the oral proceedings of 14 March 2013 and a description to be adapted thereto.

The Registrar: The Chairman:

K. Boelicke F. Edlinger

Decision electronically authenticated