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Datasheet for the decision of 5 November 2013

Case Number: T 1008/09 - 3.4.03

Application Number: 04755988.5

Publication Number: 1631989

IPC: H01L29/49, H01L21/28, H01L29/10

Language of the proceedings: EN

Title of invention:
GATE-INDUCED STRAIN FOR PERFORMANCE IMPROVEMENT OF A MOS SEMICONDUCTOR DEVICE

Applicant:
Intel Corporation

Headword:

Relevant legal provisions:
EPC 1973 Art. 54, 56
RPBA Art. 13(3)

Keyword:
Novelty - main and third auxiliary request (no)
Inventive step - first and second auxiliary request (no)
Late-filed auxiliary requests - admitted (no) - request clearly allowable (no)

Decisions cited:

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Catchword:

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Case Number: T 1008/09 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 5 November 2013

Appellant: (Applicant)	Intel Corporation 2200 Mission College Boulevard Santa Clara, CA 95052 (US)
Representative:	Goddar, Heinz J. Boehmert & Boehmert Pettenkoferstrasse 20-22 80336 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 18 December 2008 refusing European patent application No. 04755988.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman:	T. Bokor
Members:	V. L. P. Frank
	S. Ward

Summary of Facts and Submissions

I. This is an appeal against the refusal of European patent application No. 04 755 988 for the reasons of added subject-matter (Article 123(2) EPC) and lack of inventive step (Article 56 EPC 1973).

II. At oral proceedings before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following:

Main request:
Claims 1 to 22, filed with letter dated 29 October 2007

First Auxiliary request:
Claims 1 to 22, filed with letter dated 29 October 2008

Second Auxiliary request:
Claims 1 to 17, filed during the oral proceedings before the Examining Division on 26 November 2008

Third Auxiliary request:
Claims 1 to 18, filed with the grounds of appeal on 2 March 2009

Fourth Auxiliary request:
Claims 1 to 22, filed with letter dated 22 October 2013

III. Claim 1 of the main request reads as follows:

"1. An apparatus comprising:
a substrate (102);
a first device over the substrate including a first gate electrode (132) over a surface of the substrate;

a second device over the substrate including a second gate electrode (130) over a surface of the substrate;
a PMOS straining layer (214) disposed over the first gate electrode of the first device; and
an NMOS straining layer (213) disposed over the second gate electrode of the second device,
wherein the NMOS straining layer induces a strain on the second device that is different than a strain induced by the PMOS straining layer on the first device characterized in that the NMOS straining layer comprises a different material than the PMOS straining layer."

Claim 1 of the 1st auxiliary request differs from claim 1 of the main request in that the following feature is appended to the claim:

"and each straining layer is confined to an area of the respective electrode."

Claim 1 of the 2nd auxiliary request differs from claim 1 of the main request in that the following feature is appended to the claim:

"and the first gate electrode is under a strain caused by thermal expansion mismatch of the PMOS straining layer and a material of the first gate electrode."

Claim 1 of the 3rd auxiliary request reads as follows:

"1. An apparatus comprising:
a substrate (102);
a first transistor device over the substrate including a first gate electrode (132) over a

surface of the substrate and a source region (204) and a drain region (204) in a first well (115) of the substrate defining a channel (492) therebetween;
a second transistor device over the substrate including a second gate electrode (130) over a surface of the substrate and a source region (203) and a drain region (203) in a second well of the substrate defining a channel (404) therebetween;
a PMOS straining layer (214) disposed over the first gate electrode of the first device;
an NMOS straining layer (213) disposed over the second gate electrode of the second device,
wherein the NMOS straining layer induces a tensile strain on the channel of the second device, the PMOS straining layer (214) induces a compressive strain on the channel of the first device and the NMOS straining layer comprises a different material than the PMOS straining layer, and
wherein respective channels define an interior of the first device and the second device and the first gate electrode and the second gate electrode are exterior to the channels and the PMOS straining layer is exterior to the first gate electrode and the channel of the first device and the NMOS straining layer is exterior to the second gate electrode and the channel of the second device."

Claim 1 of the 4th auxiliary request reads as follows:

"1. An apparatus comprising:
a substrate (102);
a first device over the substrate including a first gate electrode (132) over a surface of the substrate;

a second device over the substrate including a second gate electrode (130) over a surface of the substrate;
a PMOS straining layer (214) disposed over the first gate electrode of the first device, wherein the PMOS straining layer is operable to place a strain on a lattice of the first gate electrode that is less than 10 percent; and
an NMOS straining layer (213) disposed over the second gate electrode of the second device, wherein the NMOS straining layer is operable to place a strain on a lattice of the second gate electrode that is less than 10 percent, wherein the NMOS straining layer induces a strain on the second device that is different than a strain induced by the PMOS straining layer 1 [sic] on the first device and wherein the NMOS straining layer comprises a different material than the PMOS straining layer."

IV. The following documents are mentioned in this decision:

D1 = "Novel Locally Strained Channel Technique for High Performance 55nm CMOS", K. Ota et al, International Electron Devices Meeting 2002, IEDM Technical Digest, San Francisco, CA, Dec 8-11, 2002, New York, NY: IEEE, US, 8 December 2002, pp. 27-30

D6 = US 6 573 172 B

D7 = US 2003/0040158 A

V. The examining division essentially argued that:

- The apparatus of claim 1 of the main request differed from the apparatus disclosed in document D6 in that: the NMOS straining layer comprised a different material than the PMOS straining layer. The objective technical problem could be considered as adjusting the strain of the gates to desired values. The solution proposed in claim 1 of the main request was not considered as involving an inventive step, since D6 disclosed that in order to improve the performance of a combination of a PMOS and an NMOS transistors a tensile film had to be formed over the PMOS transistor to cause compressive stress in the PMOS channel whereas a compressive film had to be formed over the NMOS transistor to cause tensile stress in the NMOS channel. In the field of semiconductor processing and microelectronic technology, strain generated by stress was a well known property of the various thin films used during the manufacturing of a semiconductor device. Document D6 disclosed exemplarily the use of silicon nitride as a straining layer for a polysilicon gate. However, other materials were well known to the skilled person to be capable of generating strain on a silicon layer. Therefore, once the material for the gate electrode was established, the skilled person was perfectly aware of what kind of materials he had to choose in order to induce the desired stress in the channel device. Hence, faced with the above objective technical problem the skilled person would, only on the basis of the common general knowledge and without the involvement of any inventive activity, choose different materials for the NMOS and the PMOS straining layers in order to adjust the strain to the desired values.

- The subject-matter of claim 1 of the first auxiliary request contained amendments extending beyond the content of the application as filed, contrary to Article 123(2) EPC. The amendment concerned was the specification that each straining layer was confined to an area of the respective electrode. This amendment was, however, not directly and unambiguously derivable from the original application documents. Figure 2 did not disclose whether the straining layer was actually confined to the area of the electrode and paragraph [0063] of the description referred to a precise straining material, ie silicon alloy formed through Type I selective epitaxial deposition.

- The apparatus of claim 1 of the 2nd auxiliary request differed from the apparatus disclosed in document D6 in that:

  a) the NMOS straining layer comprised a different material than the PMOS straining layer; and,

  b) the first gate electrode was under a strain caused by a thermal expansion mismatch of the PMOS straining layer and a material of the first gate electrode.

  The first difference, ie point (a), was the same as the one of the main request and therefore the same reasoning applied.
  As far as the difference of point (b) was concerned, saying that in an apparatus a "gate electrode is under strain caused by thermal expansion mismatch" was tantamount to defining the

apparatus in terms of its manufacturing process. In terms of apparatus features this could only mean that the PMOS straining layer and the material of the first gate electrode had different elastic coefficient tensors, which was implicit from the fact that they were different materials. Therefore the apparatus of claim 1 of the 2nd auxiliary request did not involve an inventive step.

VI. The appellant applicant essentially argued as follows:

- The apparatus of claim 1 of the main request required that the NMOS straining layer was made of a different material than that of the PMOS straining layer. In documents D6 and D7, however, both straining layers were made of the same material, namely silicon nitride, although deposited using different deposition parameters. In particular, D6 disclosed that the substrate was heated during deposition of one of the straining layers and this resulted in thermal expansion of the substrate. It was argued therefore that it was the thermal mismatch of both layers when cooled down to room temperature that produced the stress on the gate electrode. Although D7 disclosed different deposition processes for both silicon nitride straining layers, both layers were referred to as SiN_x without giving details of their exact composition. There was thus no direct and unambiguous disclosure in these documents that different materials were used for the NMOS and PMOS straining layers.

- Claim 1 of the 1st auxiliary request further required that the straining layer was confined to

an area of the respective electrode. From figures 1 and 2 of the application, it could be seen that the straining layers did not project about the margin of the respective gate electrodes. Thus, a skilled person could see from the figures that each straining layer was confined to the area of the respective electrode at least in the cross section shown of this figure. Moreover, the application as originally filed disclosed in paragraph [0063]: "silicone [sic] alloy deposition would be occurring only on the gate material(s) within the openings of the oxide film, and minimal, if any, grows on the oxide". From the word "only", a skilled person would directly discover that the silicon alloy was not only constrained in the cross sectional view as shown in figure 2, but also in the other directions. The examining division concluded that paragraph [0063] merely referred to one specific embodiment of a straining layer, namely the material silicon alloy, and thus did not allow a generalization of the disclosed feature to other materials which were covered by claim 1 on the grounds that this would represent an inadmissible intermediate generalization. However, the description disclosed a plurality of suitable materials which could be used as a material for building the straining layer (see eg paragraph [0065]).

- The apparatus of claim 1 of the 1st auxiliary request differed from those disclosed in documents D6 or D7 in that the straining layer was confined to the gate electrode. D6 and D7 disclosed instead a straining layer covering the whole transistor devices. Thus the straining layers were not flat and could not apply an homogeneous stress on the

underlying layers. The objective technical problem could therefore be regarded as providing a structure whose effects could be predicted in a more reliable manner. None of the prior art documents addressed this problem nor suggested a solution to it.

- Claim 1 of the 2nd auxiliary request required in addition to the features of claim 1 of the main request that the PMOS gate electrode was under strain caused by thermal expansion mismatch of the straining layer and the gate's material. In contrast document D6 did not disclose any heating of the substrate when the PMOS straining layer was deposited, this was done only when depositing the NMOS layer. Hence in D6 the strain of the PMOS gate electrode was not caused by thermal mismatch. The technical effect of the above feature was that the stress caused by the straining layer on the electrode could be varied in a wide range only by using different temperatures for applying the straining layer. Thus, the objective technical problem could be considered as providing an apparatus which allowed adjusting the strain to the gates to a desired value. Document D6 did not address the thermal mismatch issue and did not disclose any deposition temperatures.

- The apparatus of claim 1 of the 3rd auxiliary request defined a spatial relationship between the channels, the gate electrodes and the straining layers. In particular, the straining layer was prohibited from being on the substrate above the source or the drain regions. If the straining layer was above the source or the drain regions, the straining layer could not be said to be

exterior to the gate electrode. The prior art documents cited by the examining division did not suggest this spatial relationship between the straining layer and the source and the drain regions, and this feature furthermore differentiated the claimed apparatus from apparatuses in which the straining layer was an integral part of the gate electrodes.

- The 4th auxiliary request was filed as a reaction to the communication of the Board, annexed to the summons to oral proceedings, which raised for the first time an objection of lack of novelty on the apparatus of claim 1 of the main request. It had thus to be considered admissible, since it was a valid reaction to a newly raised objection. The added feature limited the strain of the gate electrode to be less than 10%. The inventors had found that if a strain was greater than 10%, there might be significant dislocations in the gate electrode material when brought into contact with the straining layer. None of the cited prior art documents disclosed the amount of strain produced in the gate electrode.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request - Novelty*

2.1 It is common ground that document D7 discloses a CMOS device 50 comprising a p-channel MOSFET (PMOS) and an n-channel MOSFET (NMOS), wherein straining layers 14

and 16 are disposed respectively over the NMOS and the PMOS transistors (Figure 2, ([0002], [0083]-[0089]). The straining layers 14 and 16 are both formed of silicon nitride (SiN_x) ([0088]-[0089]).

2.2 The appellant applicant argued that the apparatus of claim 1 differed from the conventional apparatus disclosed in D7 in that the NMOS straining layer comprised a different material than the PMOS straining layer.

2.3 According to document D7 both silicon nitride layers were however formed using different processes. The straining layer 14 was formed by a LPCVD (low pressure chemical vapour deposition) process ([0102]), whereas the straining layer 16 was formed by a PECVD (plasma enhanced chemical vapour deposition) process ([0104]). In the PECVD process, hydrogen is introduced into the film 16 and as a result, an actual compressive stress is generated in the film ([0104]). On the other hand, the silicon nitride layer 14 formed by the LPCVD process has an actual tensile stress ([0088]). Hence both straining layers have not only different physical properties, but also different chemical compositions.

2.4 Hence the straining layers 14 and 16 of D7 cannot be considered as being formed from the same material. It follows that in D7 the NMOS straining layer 14 comprises a different material than the PMOS straining layer 16 as required by claim 1 of the main request.

2.5 The Board judges therefore that the apparatus of claim 1 of the main request is not new within the meaning of Article 54 EPC 1973. The main request is thus not allowable.

3. *1st auxiliary request*

3.1 Claim 1 of the 1st auxiliary request differs from claim 1 of the main request in that it further requires that each straining layer is confined to an area of the respective electrode.

3.2 The examining division found in their decision that this feature was not directly and unambiguously derivable from the application as filed. The Board shares these doubts. However, this issue may be left unanswered, as the Board comes to the conclusion that the device of claim 1 does not involve an inventive step for the following reasons.

3.3 Document D7 discloses that the straining layers 14 and 16 extend over the whole area of the NMOS and PMOS transistors (Figure 2, [0035]). According to this document it had been found that in the conventional CMOS devices a compressive stress was applied to the channel regions of the n- and p-channel MOSFETs, degrading the electron mobility in the NMOS transistor ([0015]). It was thus the aim of D7 to improve the electron mobility in the NMOS transistor and to reduce the bend or warp of the semiconductor substrate caused by the other layers forming the device ([0019]-[0020]). Forming a silicon nitride (SiN_x) layer having a tensile stress over the NMOS transistor reduced the compressive stress existing in the channel region, enhancing the electron mobility in the channel ([0031]). The presence of both SiN_x layers reduced the substrate's bending, improving its flatness and making photolithographic processes easier to perform ([0032]).

3.4 The appellant applicant argued that confining the straining layer only to the transistor's gate electrode

resulted in an homogeneous stress on the underlying layers, ie the channel region. Hence, it rendered the properties of the device easier to predict.

3.5 It is established jurisprudence that the technical problem addressed by an application can be reformulated when more pertinent prior art documents are considered. However, the newly formulated technical problem has to be derivable from the application as filed or from the prior art documents. In the present circumstances however the Board is not persuaded that the technical effect alleged by the appellant can be derived from the application documents or from the prior art. To the contrary, document D7 explicitly discloses that formation of the straining layers on the area of the transistors improved the flatness of the substrate, as it compensated the stress introduced by the other layers and implanted regions forming the CMOS device, while the application does not disclose any technical effect associated with confining the straining layers to the area of the gate electrode (Figure 2 and [0063], [0065]). Hence the Board does not consider that the technical problem suggested by the appellant can be accepted and considers that the technical problem has to be reformulated in a more general, less ambitious manner, namely to provide an alternative to the structure of D7.

3.6 Document D1 discloses a CMOS device in which strain is introduced in the n-channel region by forming compressively strained polycrystalline Si gate electrodes ("Introduction"). Hence the straining layer is the gate electrode itself and is necessarily confined to the area of the gate electrode.

3.7 Thus, having regard in particular to the embodiment of document D1, the skilled person would have considered confining the straining layers of D7 to the area of the gate electrode to be a viable alternative, as the desired effect, namely to strain the channel region to affect its electron mobility, is achieved by straining the gate electrode and not by straining the remaining structure. The stress applied on the remaining structure, introduced by the nitride layers covering the whole area of the transistors, is not for straining the channel region, but for avoiding the bending of the substrate. If this additional effect is neglected, there are no reasons to extend the straining layer over the whole transistor structure.

3.8 The Board judges for the above reasons that the apparatus of claim 1 of the 1st auxiliary request does not involve an inventive step within the meaning of Article 56 EPC 1973. The 1st auxiliary request is thus not allowable.

4. 2nd auxiliary request

4.1 Claim 1 of the 2nd auxiliary request differs from claim 1 of the main request in that it further requires that the first gate electrode is under a strain caused by thermal expansion mismatch of the PMOS straining layer and a material of the first gate electrode.

4.2 The appellant applicant argued that the technical effect of the above feature was that the stress caused by the straining layer on the electrode could be varied in a wide range only by using different temperatures for applying the straining layer, since the amount of applied stress only depended on the difference between

the deposition temperature and the working temperature, usually room temperature.

4.3 Document D6 discloses a CMOS device in which first 130 and second 150 silicon nitride straining layers are applied respectively on the whole area of the PMOS 104 and NMOS 102 transistors (column 6, line 12 to column 7, line 22, Figure 2). The first nitride layer 130 is created in a PECVD process without any heater block power applied to the substrate (column 4, line 64 to column 5, line 10). The second nitride layer 150 is also created in a PECVD process while applying 400-500W low frequency RF heater block power to the substrate (column 5, lines 50-67). Hence the second nitride layer is applied on a heated substrate. Stress is applied to the gate electrode upon cooling to room temperature, due to the difference in the thermal expansion coefficient of polysilicon, the gate electrode's material, and silicon nitride. Whether a tensile or a compressive stress is applied by the straining layer on the gate depends on the relation between the thermal expansion coefficient of these two materials. Hence both kinds of stress, tensile or compressive, may be generated upon cooling.

4.4 The apparatus of claim 1 of the 2nd auxiliary request differs thus from the apparatus disclosed in document D6 in that:

(a) the NMOS straining layer comprises a different material than the PMOS straining layer, and
(b) the second gate electrode, ie the NMOS gate electrode, is under a strain caused by thermal expansion mismatch of the NMOS straining layer and a material of the second gate electrode.

4.5 Document D7 discloses that different materials can be used for the straining layers of the NMOS and the PMOS transistors (see point 2.3 of this decision). The skilled person is thus aware of the possibility of using feature (a) in the device of D6.

4.6 On the other hand the skilled person knows that choosing a material with a suitable coefficient of thermal expansion allows him to apply the desired stress, namely tensile or compressive, on the NMOS or the PMOS gate electrode. This have been done in the PMOS transistor of D6.

4.7 Hence the Board concludes that combining measures (a) and (b) mentioned above results in choosing the appropriate material for the straining layers on the basis of their lattice spacing and/or their thermal expansion coefficient, ie values that are well known by the skilled person in the field of semiconductor devices. Furthermore the application does not disclose any technical effect that results from applying a straining layer with thermal mismatch on the NMOS transistor instead of on the PMOS transistor, as done in D6. Hence choosing the NMOS transistor instead of the PMOS transistor may confer novelty over D6, but does not involve an inventive step.

4.8 The Board judges for the above reasons that the apparatus of claim 1 of the 2nd auxiliary request does not involve an inventive step within the meaning of Article 56 EPC 1973. The 2nd auxiliary request is thus not allowable.

5. 3rd auxiliary request

5.1 Claim 1 of the 3rd auxiliary request defines the spatial relationship between the gate electrodes (over the substrate), the channels (in a well of the substrate) and the straining layers (over the gate electrode), whereby

(a) the channels define respectively an interior of the NMOS and the PMOS device,
(b) the gate electrodes are exterior to the respective channels and
(c) the straining layers are exterior to the respective gate electrodes and channels.

Claim 1 further requires that the NMOS straining layer comprises a different material than the PMOS straining layer.

5.2 The appellant applicant explained at the oral proceedings before the Board that these definitions delimited the claimed apparatus from document D1 in which the gate electrode acted simultaneously as straining layer. Thus in the case of the device of D1 the straining layer was not exterior to the gate electrode.

5.3 However, in the apparatus disclosed in document D7 the straining layers 14 and 16, apart from comprising different materials, are disposed respectively over the NMOS and the PMOS gate electrodes 6 and 13 and their corresponding channels, while the gate electrodes are overlying, ie exterior to, the channels which are formed in the respective wells 3 and 4 (Figure 2). Hence the spatial relationship specified in claim 1 of this request is fulfilled by the apparatus of D7.

5.4 The appellant also argued in his written submissions that the present formulation of claim 1 required that the straining layers were prohibited from being on the

substrate above the source and drain regions, as it was in the embodiments of documents D6 and D7.

5.5 The Board however cannot see that this limitation is derivable from the wording of claim 1. Specifying that the straining layers are exterior to the gate electrode and the channel does not imply that the straining layers are not on the substrate above the source and drain regions. In the apparatus of D7 the straining layers are also exterior to the gate electrode and the channel.

5.6 The Board judges therefore that the apparatus of claim 1 of the 3rd auxiliary request is not new within the meaning of Article 54 EPC 1973. The 3rd auxiliary request is thus not allowable.

6. 4th auxiliary request

6.1 Claim 1 of the 4th auxiliary request differs from claim 1 of the main request in that it further requires that:

(a) the PMOS straining layer is operable to place a strain on a lattice of the first gate electrode that is less than 10 percent, and that
(b) the NMOS straining layer is operable to place a strain on a lattice of the second gate electrode that is less than 10 percent.

6.2 According to Article 13(3) RPBA: "*Amendments sought to be made after oral proceedings have been arranged shall not be admitted if they raise issues which the Board or the other party or parties cannot reasonably be expected to deal with without adjournment of the oral proceedings.*"

6.3 The 4th auxiliary request was filed with letter of 22 October 2013, ie after oral proceedings had been arranged, and thus Article 13(3) RPBA has to be considered.

6.4 The present application deals with the application of stress on the gate electrode to strain the channel of a MOS transistor, altering thus the electron mobility in the channel. This is achieved by placing a straining layer on top of the gate electrode. For the first time with this request a specific value has been specified in the claims setting an upper limit of 10% to the strain of the gate electrode. The Board has doubts however that this specific value was searched, since it was not specified in any of the original claims and was not presented as having any particular significance in the application. The Board also notes that the measurement method for determining the strain in a gate electrode of a MOS transistor, ie a device in the micrometer or even submicrometer range, has not been disclosed in the application, since the application merely discloses that *"In one embodiment, the strain is less than about 10%"* without giving any indications on how this value was determined ([0031]). Last but not least, the Board considers it part of the general knowledge of the skilled person in the field of semiconductor devices that dislocations occur in a crystalline material when too much strain is applied to its lattice. Hence it would have been obvious to the skilled person to limit the strain in order to prevent dislocations. It follows that the 4th auxiliary request is far from being clearly allowable, as several new issues arise in connection with claim 1. Moreover, it cannot reasonably be expected that the Board would have been in a position to deal with these issues without adjournment of the oral proceedings.

6.5 The appellant applicant argued that this request had been filed in view of the Board's preliminary opinion that claim 1 of the main request lacked novelty.

6.6 The Board does not find this argument to be convincing, since the claims of the 1st and 2nd auxiliary requests overcame already the Board's objection of lack of novelty by adding further features to claim 1 of the main request.

6.7 The Board decides for these reasons to not admit the 4th auxiliary request into the proceedings according to Article 13(3) RPBA.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero T. Bokor

Decision electronically authenticated