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Datasheet for the decision of 18 October 2011

Case Number: T 0448/09 - 3.4.01

Application Number: 96202805.6

Publication Number: 768538

IPC: G01R 31/3185, G06F 11/267, G11C 29/00

Language of the proceedings: EN

Title of invention:
Method and tester for applying a pulse trigger to a unit to be triggered

Patentee:
JTAG Technologies B.V.

Opponent:
Firma Göpel electronic GmbH

Headword:
-

Relevant legal provisions (EPC 1973):
EPC Art. 54, 56

Keyword:
"Novelty (yes)"
"Inventive step (yes)"
"Apportionment of costs (no)"
"Devolutive effect of the appeal"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0448/09 **-** 3.4.01

D E C I S I O N
of the Technical Board of Appeal 3.4.01
of 18 October 2011

Appellant: (Patent Proprietor)
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Decision under appeal:
Interlocutory decision of the Opposition Division of the European Patent Office posted 5 December 2008 concerning maintenance of European patent No. 768538 in amended form.

Composition of the Board:

Chairman: H. Wolfrum
Members: P. Fontenay
G. Weiss

Summary of Facts and Submissions

I. The appeal lies from the interlocutory decision of the opposition division to maintain European patent No. EP-B-768 538 in amended form according to the second auxiliary request filed by the patentee during the oral proceedings before the opposition division on 13 October 2008. The decision was announced during the oral proceedings and dispatched on 5 December 2008.

In its decision, the opposition division held that the subject-matter of claim 1 of the main request and first auxiliary request lacked novelty in view of user manual "ASP 100-D/PROG" (D28), dated 10 September 1994 and delivered by the opponent with the corresponding equipment prior to the priority date claimed for the present patent. Furthermore, a decision of apportionment of costs was taken by the opposition division on the request of the patentee.

II. The appellant (patentee) filed an appeal against said decision by facsimile dated 13 February 2009 and paid the prescribed appeal fee on the same day. In the notice of appeal, the appellant requested that the decision to refuse maintenance of the patent in amended form on the basis of the main request or first auxiliary request filed in the course of the opposition proceedings on 12 September 2008 be overturned.

In the statement setting out the grounds of appeal, filed on 15 April 2009, the appellant requested that the patent be maintained in amended form on the basis of claims 1-4 according to a main request or, in the alternative, on the basis of claims 1-4 according to a

first, a second or a third auxiliary request or, on the basis of claims 1-3 according to a fourth auxiliary request. The main request and the second and fourth auxiliary requests corresponded, respectively, to the main request and the first and second auxiliary requests underlying the decision in suit. On the other hand, the appellant requested to maintain the decision with respect to the apportionment of costs and the request for fixing costs as referred to in paragraph 5 of the interlocutory decision.

A copy of a document cited in the original patent application to illustrate the concepts of Boundary Scan Test (D35) was also filed in support of the appellant's argumentation.

III. In a facsimile of 11 September 2009, the respondent (opponent) requested that the appeal be dismissed and that the appellant be charged the costs incurred by the respondent with regard to the late filing of document D35.

Both parties requested that oral proceedings be held in the case that the Board did not intend to grant their respective main requests. Summons were accordingly issued on 2 May 2011.

IV. On 22 June 2011 the Board issued a communication pursuant to Article 15(1) Rules of Procedure of the Boards of Appeal (RPBA), expressing its provisional opinion with regard to the requests then on file.

It was, in particular, stressed that an essential aspect to be clarified during the oral proceedings

concerned the definition of the terms "Boundary Scan" and "Boundary Scan Test" which appeared in the independent claims of all requests.

The Board further indicated that, according to its provisional opinion, it could not find fault in the finding of the opposition division according to which the circuit disclosed in prior art document D28 contained a pulse circuit, contrary to the view defended by the appellant.

These two aspects were considered essential when deciding on the novelty of the subject-matter of claims 1 and 3 of the main request in view of the system disclosed in Figure 3 of document D28.

Concerning the first, second and third auxiliary requests, the Board expressed doubts as to their allowability under Article 123(2) EPC in view of the amendments which had been carried out.

With respect to the appellant's fourth auxiliary request, it was noted that, the patentee being sole appellant against the interlocutory decision of the opposition division maintaining the patent on the basis of this request, the doctrine of *reformatio in peius* applied and forbade that this request be examined by the Board.

V. The oral proceedings were held on 18 October 2011, both parties being represented.

In the course of the oral proceedings, the appellant requested that the decision under appeal be set aside

and that a patent be maintained in amended form on the basis of claims 1 and 2 according to the main request filed at the oral proceedings, replacing the former main request filed on 15 April 2009. The first to third auxiliary requests, as filed on 15 April 2009, were maintained. Moreover, the fourth auxiliary request to maintain the patent in amended form on the basis of claims 1-3 according to the second auxiliary request referred to and attached to the interlocutory decision in opposition proceedings dated 5 December 2008 was maintained. Finally, the appellant requested to maintain the decision with respect to the apportionment of costs and the request for fixing costs as referred to in paragraph 5 of the interlocutory decision in opposition proceedings dated 5 December 2008.

In the oral proceedings, the respondent (opponent) confirmed its request that the appeal be dismissed and that the appellant be charged of the costs incurred by the respondent with regard to the late filing of document D35. No objection as to the admissibility of the appellant's new main request was raised.

VI. The following documents were more particularly considered in the course of the appeal procedure:

D2: IEEE standard 1149.1-1990, "IEEE Standard Test Access Port and Boundary-Scan Architecture", cited in the patent description, Copyright 1990;

D15: J. Coleman et al. "Boundary Scan Speeds Static Memory Tests" in Electronic Design, Vol. 41, (1993), February 18, No.4, pages 61-73;

D16: Göpel electronic: "ASC 16 Benutzerhandbuch", a user manual dated June 1994;

D19: R. Lindner: "Eidesstattliche Versicherung" dated4 February 2002;

D20: G. Becke: "Scope™ Octals, Application, Architecture and Function", December 1991, Rev.: 1.0 in Texas Instruments: "Scope™ Logic Products, Application and Data Manual", 1994;

D27: Göpel electronic: document relating to the delivery of an ASP 100-D/PROG and 4 user manuals for ASP 100-D/PROG to LIF ELEKTRONIK A/S, dated 13 September 1994;

D28: N. Münch et al.: "ASP 100-D/PROG User Manual", printed 13 September 1994;

D29: Göpel electronic: "MFC 1149.1 Benutzerhandbuch", a user manual dated December 1991;

D30: Göpel electronic: document relating to the delivery of three MFC 1149.1-B and one ASP 100-D/PROG to LIF ELEKTRONIK A/S, dated 1 August 1994;

D32: Confirmation of use of a MFC 1149.1 plug-in card with attached ASP 100-D/PROG hardware and associated software in 1994 at Dancall Telecom A/S by Mr. S. M. Larsen; document further including as enclosure the corresponding User Manual (D28);

D33: Confirmation of use of a MFC 1149.1 plug-in card with attached ASP 100-D/PROG hardware and associated software in 1994 at Dancall Telecom A/S by Mr. T. Hollesen; document further including as enclosure the corresponding User Manual (D28);

D34: Confirmation by Mr. W. Grösch and Mr. T. Dombrowski of delivery by Göpel electronic GmbH to BOSCH Telecom in June 1995 of a "Boundary Scan Testsystem" with a copy of some pages of the "User Manual Cascon - Galaxy" delivered together with the test System;

D35: Philips Test and Measurement; "The ABCs of Boundary-Scan Test"; a document printed in the USA without indication of date;

D36: Philips Test and Measurement; "The ABC of Boundary-Scan Test"; a document printed in the Netherlands without indication of date.

For the submissions of the parties reference is made to the reasons of present decision.

VII. Claim 1 of the main request reads as follows:

"*1. A method of applying a pulse trigger to a unit (108) that is to be triggered during a Boundary Scan of an electronic circuit (106) carried out by Boundary Scan Test logic and which electronic circuit (106) comprises the unit (108), the method comprising the steps of:*

determining a state in Boundary Scan Test logic in which the pulse trigger can be generated;

activating a pulse circuit (404; 806; 1004) by the Boundary Scan Test logic in response to said state; and

generating the pulse trigger by the pulse circuit (404; 806; 1004) in response to said activating step,

characterized in that said steps are performed in a tester (102) external to said electronic circuit (106) comprising said unit (108) to be triggered."

Claim 2 of the main request depends on claim 1.

The auxiliary requests differ from the main request in that claim 1 includes additional amendments and/or limitations regarding the claimed method and in that

they further include claims relating to the corresponding tester.

VIII. In this decision reference is made to the provisions of the EPC 2000, which entered into force as of 13 December 2007, unless the former provisions of the EPC 1973 still apply to pending applications, in which case the evocation of the Article or Rule is followed by the indication "1973".

Reasons for the Decision

1. The appeal meets the requirements of Articles 106 EPC, 107 EPC 1973, 108 EPC and Rule 99 EPC. It is thus admissible.

2. *Main request - Admissibility*

The Board - exercising its discretional power under Article 13(1) RPBA - decides to admit the new main request, filed during the oral proceedings, into the appeal proceedings. Although filed late, the new main request only differs from the main request filed on 15 April 2009 with the statement setting out the grounds of appeal in that claims 3 and 4 directed to a tester have been deleted. These amendments neither affect the procedural economy of the proceedings nor do they introduce any new subject-matter the complexity of which would have justified a different conclusion. Besides, the respondent did not object to the admission of the new main request.

3. *Main request - Novelty*

3.1 Documents D32 and D33 confirm the use in 1994 of a piece of equipment provided by Göpel electronic in order to program Flash devices via Boundary Scan. D32 and D33 further confirm that the user manual, referred to in these proceedings as D28 and explicitly referred to as enclosure in D32 and D33, reflects the ASP100-D/PROG state used in 1994 and describes exactly the setup which was used at that time at Dancall Telecom A/S. The appellant did not question the fact that D28 is prior art in the sense of Article 54(2) EPC 1973. The Board is thus satisfied that sufficient evidence has been provided that document D28, which bears the date of 10 September 1994, was indeed available to the public before 13 October 1995, i.e. the date of the priority claimed for the patent in suit.

3.2 D28 is a user manual describing a system and associated process for testing up to four units under test (UUT). D28 contains a more detailed description of the system when being used for programming Flash memories. In particular, Figure 3 of D28 describes the specific setup when programming FLASH-EPROMs in which the address lines are formed by Bscan-devices provided on the Unit Under Test incorporating the actual FLASH-EPROM to be programmed. According to the architecture disclosed in Figure 3, control signals and data are provided via parallel lines.

The Board concurs with the opposition division in its finding that a pulse trigger is applied to the FLASH-EPROM to be triggered. In the Board's judgement, the indication on page 15 of D28 under section

"masked_pipoutput", relating to the ability of the software extension to generate pulses in combination with the disclosed hardware, constitutes sufficient evidence of the presence of a pulse circuit reacting to a pulse trigger. The appellant's view according to which the activation of the pulse circuit in D28 would not constitute a response to the state identified in the Boundary Scan Test logic and that the cause/effect relationship would thus be missing is not shared by the Board. In this respect, the Board notes that the sentence: "*Then, when a burst is started, the TAP state DrUpdate will be executed after a time of 6x TCK in maximum*" in the passage relating to the synchronisation of PIP outputs with the DrUpdate, on page 11 of D28, indeed implies the existence of such a causal link. Furthermore, as illustrated in Figure 3, the various steps referred to above are performed in a tester external to the electronic circuit comprising the unit to be triggered (the FLASH-EPROM). More specifically, these steps are carried out by the combination of the probe ASP 100-D/PROG in combination with the Boundary Scan Test-hardware ASC or MFC 1149-1 as disclosed in documents D16 or D29, respectively, together with the CASCON software package.

3.3 As a consequence, the novelty of the claimed method hinges solely on the question whether the method disclosed in document D28, which makes use of a Boundary Scan solely for the address data, really defines a "Boundary Scan of an electronic circuit carried out by Boundary Scan Test logic" as recited in claim 1. In the appellant's view, the concepts of "Boundary Scan" and "Boundary Scan Test" had a recognised meaning in the art and referred to well-

defined techniques which implied that each of the I/O pins of the electronic circuit to be tested be connected to a cell within a Boundary Scan register. By contrast, the opposition division held that these notions merely implied that some I/O pins of the electronic circuit were connected to a chain of Boundary Scan Cells, as put forward by the opponent. The expression "partial Boundary Scan" was used by the opposition division to define this latter configuration and associated technique. The Board has, thus, to decide whether a "partial Boundary Scan" indeed defines a Boundary Scan in the sense of the present patent specification.

3.3.1 As may be derivable from the paragraph in column 1, lines 25-33, of the application as published, "*Boundary Scan Test (BST) is a method developed to assist the testing of Printed Circuit Boards and is laid down in a standard (IEEE Std. 1149.1 - 1990). The BST method is also described in U.S. Patent No. 5,430,735 (PHN 11.856). The publication "The ABCs of Boundary Scan Test", published by Philips Test & Measurement, Eindhoven, the Netherlands, describes the concept of the method and contains examples of its implementation*". The standard IEEE 1149.1 - 1990 corresponds to document D2, while documents D35 and D36, cited by the appellant and respondent, respectively, describe two slightly different versions of a booklet meant to give a first insight into Boundary Scan Test technology for the testing of Printed Circuit Boards. D35 and D36 were, respectively, published in the USA and The Netherlands, wherein the latter bears the title "The ABC of Boundary-Scan Test" (without an "s" at ABC). Both documents, as well as many other documents of the prior

art cited in the course of the present opposition proceedings, refer to the norm 1149.1 - 1990 (cf. e.g. D35, page 4; D36, page 5) which constitutes the reference document in the field of Boundary Scan testing and thus defines the essential concepts inherent to this technology.

In the respondent's opinion, the strict interpretation of the term "Boundary Scan" relied on by the appellant by reference to document D2 should be rejected since such an interpretation would be inconsistent and conflict with the actual teaching of the present patent specification. In this respect, particular emphasis was put on the general overview of the operation of a component compatible with the standard IEEE 1149.1 - 1990 provided in paragraph 1.2, on page 1-1 of D2, according to which "*All information (instruction, test data, and test result(s) is communicated in a serial format*". In the respondent's opinion, the embodiments of the claimed invention are in direct contradiction to this specification since the trigger pulse was transmitted in parallel.

3.3.2 In the Board's judgement, the present invention nevertheless fulfils the requirements of this standard. It is observed, in this context, that the standard itself makes a distinction between "rules", "recommendations", and "permissions" (cf. D2, page 2-1, section "Specification"). According to this distinction, "*Rules specify the mandatory aspects of this standard. Clauses that are rules contain the word shall*". Moreover, Rule (a) in Chapter 12, "Conformance and Documentation Requirements" (cf. D2, page 12-1) which reads: "*Components that claim conformance to this*

standard shall comply with all relevant rules in the Specifications subsections of this standard.", clearly makes conformity to the standard dependent on specific requirements, namely those defined as "Rules". As a consequence, the general overview in paragraph 1.2 on page 1.2 of D2 relied on by the respondent with regard to the communication of all information in a serial format does not constitute, in the absence of any corresponding rule, a prerequisite for the compatibility of a component or device with said standard. Similarly, the fact that more than four lines are provided according to the embodiments of the present invention to transmit information required for the tests to be carried out does not appear to contradict any of the rules of the standard. More generally, the respondent was not able to provide evidence that any of the rules referred to in Standard 1149.1 - 1990 was infringed by the embodiments of the invention described in the present patent.

It is further stressed that the requirement defined in Rule (a) of Chapter 10: "The Boundary-Scan Register", on page 10-1 of D2, according to which "*Boundary-scan register cells shall be connected between each digital system pin and the on-chip system logic to allow the state of the system pin and, where appropriate, the system logic connection to be controlled or observed or both*" is indeed fulfilled by the functional unit constituted by the combination of the components 114, 118, 122 and 108 in the present patent specification (cf. published patent specification, column 3, lines 4-17).

As a matter of fact, although document D2 defines a standard applying, primarily, to Boundary-Scan architectures, it also indirectly defines methods associated to these technologies, as for example confirmed by the statement in the sixth paragraph of page 1-3 in D2 which reads: "***1.3.2 What is Boundary Scan?*** [bold in the text] *The boundary-scan technique involves the inclusion of a shift register stage (contained in a boundary-scan cell) adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles*". The explicit reference in paragraph [0003] of the patent specification to the method laid down in the standard IEEE 1149.1 - 1990 confirms that the method according to the invention is to be understood in the light of the testing methods operated on devices underlying this standard.

3.3.3 In contrast to this, the respondent stressed the point that the standard IEEE 1149.1 - 1990, as compiled in document D2, did not pertain to the method of Boundary Scan testing as such but only imposed rules to be met by the structure of electronic circuits so as to be amenable to Boundary Scan testing. The mere fact that the standard evoked, in passing, Boundary Scan techniques did not affect this finding. Therefore, the said standard had no bearing on a method employing Boundary Scan testing such as defined by claim 1 of the main request under consideration.

Although the Board agrees with the respondent as regards the actual scope of the said standard, it does not concur with the respondent's conclusions as to the standard's consequences for the method as claimed by

claim 1 of the main request. The circuit under test according to document D28 is simply not designed for a Boundary Scan Test on all of its components. Due to the fact that the control pins and the data pins are tested by applying test signals via parallel data lines, the circuit under test complies only in part with the standard IEEE 1149.1 - 1990 and the testing method taught by document D28 thus relates to a mixed testing method, of which only a part constitutes a Boundary Scan Test. It follows that the testing method disclosed in document D28 does not correspond to a "Boundary Scan of an electronic circuit carried out by Boundary Scan Test logic" in the sense of the present patent specification.

3.3.4 None of the other cited prior art documents discloses the step of applying a pulse trigger to a unit to be triggered during a Boundary Scan of an electronic circuit in which the chain of Boundary Scan cells interfaces each I/O pin of the electronic circuit with the unit to be triggered, as implied by claim 1 of the main request when construed in the light of the IEEE 1149.1 - 1990 standard. The claimed method is therefore new in the sense of Article 54 EPC 1973.

4. *Main request - Inventive step*

The problem of long processing times when applying a pulse trigger during Boundary Scan Testing is known from the prior art and is, for example, explicitly acknowledged in document D15 (cf. D15, page 61, fourth paragraph). However, contrary to the respondent's submission, this problem does not apply to the testing configuration defined in Figure 3 of D28. In fact, as

convincingly observed by the appellant, the configuration of Figure 3, with the control and data signals being provided in parallel, permits to generate the pulse trigger whenever required without recurring to the time consuming process of vectors being shifted through the Boundary Scan register. As a matter of fact, the problem defined above does not appear to reflect the actual difference which exists between the claimed method and the testing method apparent from document D28. According to the well-established problem-solution approach developed by the EPO, in order to decide on the inventive merits of a claimed invention, the objective problem should directly derive from the features which distinguishes the claimed invention from the prior art.

In the present case, the claimed method differs from the method of D28 in that the pulse trigger is applied to a unit to be triggered during a Boundary Scan of an electronic circuit implying, according to the definition retained above under section 3, that a cell in a chain of Boundary Scan cells interfaces each I/O pin of the electronic circuit with the logic of the unit to be triggered.

This distinguishing feature permits to address each pin of the electronic circuit via the Boundary Scan path, i.e. via a Boundary Scan architecture specified in the standard according to document D2, wherein test signals are applied in a serial manner to the chain of Boundary Scan Test cells via a test access port (TAP).

The problem solved by the claimed invention thus consists in allowing for Boundary Scan Testing

(implying sticking to the architecture of the TAP port as defined in standard D2) while speeding up the testing process.

While it may indeed be envisaged to modify the configuration disclosed in Figure 3 of D28 so as to transmit all information (addresses, instructions and data) via the TAP port, this approach would lead the skilled person to speed up the testing process on the basis of the data actually available in the electronic circuit, i.e. on the basis of the data contained in the Boundary Scan register of said circuit. This would further lead the skilled person to privilege solutions in which the logic of the pulse circuit would be controlled by Boundary Scan cells within the Boundary Scan register in the electronic circuit, thus leading to solutions of the kind illustrated in Figures 2 and 3 of the original application where the determination of a state in which a pulse trigger can be generated, as well as the activation of the pulse circuit and the generation of the pulse trigger, are performed within the electronic circuit, contrary to the claim's wording.

In this respect, the alternative solution consisting of transmitting most of the information via the TAP port while keeping the parallel control line of Figure 3 in D28 for transmitting the pulse trigger would result from hindsight considerations. This is all the more true as the skilled person would recognise that the solution evoked above is fully satisfactory in view of the objective problem to be solved and that the alternative solution would actually jeopardise the

advantage conferred by the system of D28 in terms of speed of testing.

For these reasons, the Board concludes that the method of claim 1 of the main request does not result in an obvious manner from the teaching of document D28. Its subject-matter is therefore inventive in the sense of Article 56 EPC 1973.

5. *Auxiliary Requests*

Since the appellant's main request is allowable, there is no need for the Board to decide on the allowability of the first to fourth auxiliary request.

6. *Respondent's request for apportionment of costs*

Document D35 is a document which is cited in the original patent application in order to illustrate the principles of Boundary Scan Test methods. Its introduction in the appeal proceedings is considered to constitute a direct reaction to the fact that the appellant's line of argumentation, which relied on the actual definition of Boundary Scan, was unsuccessful before the opposition division. Its filing, in an attempt to reverse this adverse finding, appears therefore legitimate and can, thus, not justify an apportionment of costs in favour of the respondent.

7. *Appellant's request for maintaining the decisions with respect to the apportionment and fixing of costs.*

The appellant requested to maintain the decision with respect to the apportionment of costs and the request

for fixing costs as referred to in paragraph 5 of the interlocutory decision in opposition proceedings dated 5 December 2008. The Board, however, observes that this part of the decision of the opposition division has not been appealed. The devolutive effect of an appeal before a board extends only to the part of the impugned decision which is indicated in the notice of appeal as provided in Rule 99(1)c) EPC. This in turn implies that the part of the impugned decision not indicated in the notice of appeal becomes final on expiry of the time limit for filing an appeal and cannot later become an object of the appeal proceedings. In the present situation, the aspect of the decision relating to the apportionment of costs was not appealed and is thus res judicata. The appellant's request to maintain the decision with respect to the apportionment of costs is thus devoid of object.

Similarly, the appellant's request to maintain the decision with respect to the fixing of costs is devoid of object since no such decision has been taken so far. As specified under point 5(d) of the decision under appeal the opposition division shall, on request, fix the amount of costs to be paid under a final decision apportioning them. Although the decision concerning the apportionment of costs has become final, no request regarding the fixing of costs has yet been filed.

Order

For these reasons it is decided that:

1. The interlocutory decision of the opposition division under appeal insofar as it concerns patentability is set aside.

2. The case is remitted to the opposition division with the order to maintain the patent in amended form in the following version:
   - claims 1 and 2 filed at the oral proceedings on 18 October 2011 as main request;
   - description, columns 1 to 7 filed at the oral proceedings on 18 October 2011;
   - Figures 1 to 5 of the patent as granted.

3. The respondent's request for apportionment of costs is rejected.

The Registrar The Chairman

M. Schalow H. Wolfrum