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Case Number: T 0425/09 - 3.4.03

Application Number: 00310216.7

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Title of invention:
Organic EL display apparatus and manufacturing method thereof

Applicant:
Sony Corporation

Headword:
-

Relevant legal provisions:
EPC Art. 123(2)

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Case Number: T 0425/09 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 5 March 2013

Appellant: (Applicant)
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 26 September 2008 refusing European patent application No. 00310216.7 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: T. M. Häusser
T. Bokor

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division to refuse European patent application No. 00 310 216 for lack of lack of inventive step within the meaning of Article 56 EPC 1973.

II. At the oral proceedings before the board the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of Claims 1-6 filed under the label of "Auxiliary Request" with letter dated 5 February 2013 and amended application documents (pages 6 to 11, Fig. 1) filed with letter dated 25 February 2013, as sole request.

III. The following document is referred to in this decision:

Sketch A: appellant's drawing submitted with letter dated 21 January 2009 setting out the grounds of appeal.

IV. The wording of independent claim 1 of the sole request reads as follows (labelling "(i)" and highlighting by the board):

"A display apparatus including a substrate (1), a plurality (PXL) of pixels of upside light taking out structure formed on said substrate (1), and a barrier plate (6) for separating adjoining pixels of said pixels (PXL) from each other, wherein:

each of said pixels (PXL) comprises a lower layer portion (LL) including: a wiring formed on said substrate; a scanning wiring (X), a part of said wiring, for supplying first electric information for

selecting said pixels (PXL), a data wiring (Y), another part of said wiring, for supplying brightness information for driving said pixels (PXL); a first active element (TFT) controlled by second electric information supplied from the scanning wiring and having a function of writing the brightness information supplied from the data wiring (Y) into one of said pixels; and a second active element (TFT) having a function of controlling emission of light of said organic electro-luminescent element by supplying a current to an organic electro-luminescent element (OLED) in accordance with the written brightness information;

each of said pixels (PXL) comprises an upper layer portion (UL) including: an organic electro-luminescent element (OLED);

each of said pixels comprises a middle layer portion (ML) for electrically insulating said lower layer portion (LL) and said upper layer portion (UL) from each other;

(i) the scanning wiring extends under the organic electro-luminescent (OLED) element and the data wiring does not extend under the organic electro—luminescent (OLED) element;

said organic electro-luminescent element (OLED) is connected with the wiring through a contact hole (CON) formed in said middle layer portion (ML), and

said barrier plate (6) is disposed in said upper layer portion (UL) so as to overlap with a contact region both including the contact hole (CON) and having many undulations such that the organic electro-luminescent element (OLED) is formed as wide as possible on a comparatively flat portion except for the

contact region whereby the aperture rate of the pixel is enlarged."

V. In relation to the basis in the original application documents for feature (i) the appellant argued essentially as follows:

It was clear to the skilled person that Figure 5 gave a true representation of the circuit used in the apparatus according to the invention, namely one involving a first and a second thin film transistor (TFT). Furthermore, the only explicit statement about the TFT shown in Figure 1 was on page 9, lines 4-5, where it was mentioned that it was in fact the second TFT. Since the drain of the TFT was connected to the organic electro-luminescent element OLED, it was clear that the element labelled "Y" could not be the data wiring, which was not shown in Figure 1, but had to be the ground wiring instead. The label "Y" was therefore in error and should be deleted. Without that label there was no inconsistency between Figures 1 and 2.

Furthermore, in relation to the scanning wiring there was no inconsistency between Figures 1 and 2, either. One possibility to reconcile the Figures was that Figure 1 was an oblique section of the arrangement shown in Figure 2, leaving the OLED region just before crossing the scanning wiring. Alternatively, the scanning wiring was not shown in Figure 1 at all and the label "X" referred to something else, for example the line joining the first TFT to the gate of the second TFT.

In the description there was no explicit disclosure about the position of the scanning and the data wiring. However, from Figure 2 it was apparent that the scanning wiring extended under the OLED and the data wiring did not extend under the OLED. Feature (i) was therefore disclosed in the original application documents.

Reasons for the Decision

1. Admissibility

The appeal is admissible.

2. Amendments

2.1 Preliminary considerations

2.1.1 Feature (i) relates to the positioning of the scanning wiring and data wiring in relation to the organic electro-luminescent element OLED. As acknowledged by the appellant, there is no explicit indication in the description of the application regarding that positioning. However, in the appellant's opinion, feature (i) could be deduced in particular from Figure 2 of the application.

2.1.2 It will be of significance in the discussion below that Figures 1, 2, and 5 relate to the same apparatus. In particular, Figure 1 relates to a partial sectional view of a display apparatus; Figure 2 shows a partial plan view of that display apparatus and Figure 5 relates to a circuit diagram showing an equivalent circuit of a pixel of the display apparatus of Figure 1 (see the description of the application, page 6, lines 2-5 and 11-12). Furthermore, Figures 3 and 4A to 4C relate to further aspects concerning the apparatus according to the invention (page 6, lines 6-10 and 21-22; page 12, lines 7-8; page 13, lines 9-11).

2.1.3 As detailed in the description (see page 8, line 22 – page 9, line 3; page 16, line 16 – page 17, line 20),

in particular in relation to Figure 5, two thin film transistors TFT1 and TFT2 are used in order to control the light emission of the OLED of a pixel.

However, only one thin film transistor labelled "TFT" is shown in Figure 1. Furthermore, the description is contradictory regarding this transistor TFT:

On the one hand, from the statement that the data wiring Y is electrically connected with the source area S of the thin film transistor TFT (page 9, lines 15–18) it follows in combination with the circuit diagram shown in Figure 5 that the transistor TFT in Figure 1 is in fact the first transistor TFT1 in Figure 5.

On the other hand, from the statement that the anode A of the OLED is electrically connected with the drain area D of the thin film transistor TFT (page 9, lines 18–23) it follows in combination with the circuit diagram shown in Figure 5 that the transistor TFT in Figure 1 is the second transistor TFT2 in Figure 5. The statement that the transistor TFT is the "second active element" on page 9, lines 4–5, in combination with the passage on page 8, line 23 – page 9, line 3, leads to the same conclusion.

It will be shown below that it is not evident for the skilled person how to resolve this contradiction.

2.2 First part of feature (i)

2.2.1 In the first part of feature (i) it is specified that the scanning wiring extends under the OLED. Figure 2 shows indeed that a part of the element labelled "X",

which is described to be the scanning wiring in the description (see for example page 8, last paragraph, of the description of the application), passes under the hatched region indicating the position of the OLED.

By contrast, in Figure 1 it is shown that the element labelled "X" is *not* under the OLED. Therefore, there is an apparent contradiction between Figures 1 and 2 as to the position of the element labelled "X" in relation to the OLED.

2.2.2 The appellant argues that one possible way to reconcile Figures 1 and 2 was to assume that the section shown in Figure 1 was oblique. This meant that the section of Figure 1 intersected the line of the barrier 6 at an oblique angle and left the region of the OLED just before intersecting the element labelled "X".

The board does not consider this argument to be convincing. To begin with, an oblique section is highly unusual, especially in a layout as shown in Figure 2, where the scanning wirings X, the data wirings Y, the barrier plates 6, and the edges of the OLED regions are all either parallel or perpendicular to each other. Since a barrier plate 6 is shown in Figure 1 and in the absence of any indication to the contrary, one would therefore expect that the section shown in Figure 1 is perpendicular to the barrier plate 6. Furthermore, the labels "L" and "W" designate the aperture size of one pixel and the width of the barrier plate 6, respectively, as described on page 8, lines 10-13, of the description of the application. The fact that the labels "L" and "W" are shown in Figure 1 implies that

the section shown in Figure 1 indeed has to be perpendicular to the barrier plate 6.

2.2.3 Alternatively, the appellant argued that another way to reconcile Figures 1 and 2 was to assume that the scanning wiring was not shown in Figure 1 at all and that the label "X" in fact designated something else, for example the line joining the first TFT and the gate of the second TFT.

This argument is not considered to be convincing, either. First of all, the scanning wiring is consistently labelled "X" throughout the description of the application. Furthermore, the description as to the location of the scanning wiring (see the description of the application, page 8, lines 23 – page 9, line 3; page 9, line 27 – page 10, line 2), namely that it is in the lower layer portion LL of the pixel and that it is formed on the surface of the substrate 1 is consistent with the position of the element labelled "X" shown in Figure 1. Moreover, there is no other element shown in Figure 1 which could be regarded as the scanning wiring.

2.2.4 In view of the above the board is of the opinion that there is a contradiction between Figures 1 and 2 as to the position of the scanning wiring X in relation to the OLED: while the scanning wiring is shown to extend under the OLED in Figure 2, it follows from Figure 1 that the scanning wiring does not extend under the OLED. The location of the scanning wiring is therefore not unambiguously disclosed in these Figures.

2.2.5 Furthermore, Figure 2 is a schematic drawing. It shows the OLED region (i.e. the hatched region in Figure 2) extending symmetrically on either side almost up to the barrier plates 6. On the other hand, Figure 1 is asymmetric in this respect, showing the OLED region extending up to the barrier plate 6 merely on one side. Moreover, Figures 4A to 4C, which illustrate the manufacture of the OLED, show a considerable distance between the barrier plates 6 and the OLED region.

The values provided in the description (see page 8, lines 10-13; page 13, lines 1-8) by way of example for the width of the barrier plate 6, the interval between barrier plates 6, etc. also imply that the gap between the OLED region and the barrier plate 6 is about as wide as the barrier plate 6 itself.

Therefore, the skilled person would not regard it a feature of the disclosed apparatus that the OLED region extends over the scanning wiring almost up to the barrier plate 6 as shown in Figure 2.

2.2.6 For the above reasons, it is not directly and unambiguously derivable from the application as filed that the scanning wiring extends under the OLED (first part of feature (i)).

2.3 Second part of feature (i)

2.3.1 In the second part of feature (i) it is specified that the data wiring does not extend under the OLED. Similarly to the situation above, Figure 2 shows indeed that the element labelled "Y", which is described to be the data wiring in the description (see page 8, last

paragraph), does not pass under the hatched region indicating the position of the OLED.

On the other hand, in Figure 1 it is shown that the element labelled "Y" *does* extend under the OLED. Hence, there is an apparent contradiction in Figures 1 and 2 as to the position of the element labelled "Y" in relation to the OLED.

2.3.2 The appellant argued that the labelling "Y" in Figure 1 was wrong and the concerned element was actually the ground line; this would resolve the contradiction between Figures 1 and 2.

This is not unreasonable since the element is thicker than the scanning wiring, which does not need to sustain a large current, and would therefore apparently be able to sustain the current flowing through the OLED. Furthermore, the element would be in the correct lateral position for connection to the source area S of the transistor TFT shown in Figure 1. Such a connection would be consistent with the transistor TFT in Figure 1 being the second transistor TFT2, because – as can be seen from Figure 5 - the ground line is connected to the source area of the second transistor TFT2.

The appellant's interpretation is therefore consistent with the statements in the description implying that the transistor TFT of Figure 1 is the second transistor TFT2 in Figure 5, but is still in contradiction to the statement in the description implying that the transistor TFT of Figure 1 is the first transistor TFT1 in Figure 5.

2.3.3 However, another possibility to resolve the contradiction between Figures 1 and 2 is that Figure 2 is incomplete and does not show a protrusion of the data wiring Y parallel to the scanning wiring X in order to allow connection to the transistor TFT of Figure 1. This was in fact submitted by the appellant with his letter setting out the grounds of appeal (see the appellant's drawing labelled "Sketch A", in particular the protrusion of the data wiring Y parallel to the scanning wiring X and extending under the hatched region indicating the OLED).

This is not unreasonable, either, because the data wiring is consistently labelled "Y" throughout the description of the application and is described (see the description of the application, page 7, lines 1-3; page 10, lines 22-25) to be located in the lower layer portion LL of the pixel and to be formed on the interlayer isolation film 33. This is consistent with the position of the element labelled "Y" shown in Figure 1.

Furthermore, the element is in the correct lateral position for connection to the source area S of the transistor TFT shown in Figure 1. Such a connection is in fact described on page 9, lines 15-18, and implies that the transistor TFT in Figure 1 is in fact the first transistor TFT1 in Figure 5 (see point 2.1.3 above).

Even though this interpretation is consistent with the statement in the description implying that the transistor TFT of Figure 1 is the first transistor TFT1 in Figure 5, it is still in contradiction to the

statements in the description implying that the transistor TFT of Figure 1 is the second transistor TFT2 in Figure 5.

2.3.4 In view of the above it is not evident for the skilled person how to resolve the contradictions between Figures 1 and 2 concerning the element labelled "Y" and the contradictions in the description concerning the thin film transistor TFT. Furthermore, one of the possible solutions of the first contradiction, namely the one explained under point 2.3.3 above, entails that the data wiring does extend below the OLED. Therefore, it cannot be considered to be directly and unambiguously disclosed that the data wiring does *not* extend under the OLED (second part of feature (i)).

2.4 For these reasons feature (i) of claim 1 is not directly and unambiguously derivable from the application as filed. Therefore, the subject-matter of claim 1 extends beyond the content of the application as filed contrary to the requirements of Article 123(2) EPC.

3. Conclusion

In view of the above the sole request is not allowable. Therefore, the appeal has to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson