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Datasheet for the decision of 12 October 2012

Case Number: T 0318/09 - 3.5.02

Application Number: 97904231.4

Publication Number: 897616

IPC: H03L 1/02, H03L 7/06, H03L 7/16, H03L 7/18

Language of the proceedings: EN

Title of invention:
Frequency synthesizer with temperature compensation and frequency multiplication and method of providing the same

Applicant:
Wi-LAN Inc.

Headword:
-

Relevant legal provisions:
EPC Art. 111(1)

Keyword:
"Decision re appeals - new prior art document - remittal (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0318/09 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 12 October 2012

Appellant: (Applicant)
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Representative:
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 15 July 2008 refusing European patent application No. 97904231.4 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: M. Ruggiu
Members: M. Léouffre
W. Ungler

Summary of Facts and Submissions

I. The applicant lodged an appeal against the decision of the examining division, posted 15 July 2008, to refuse the application. The statement setting out the grounds of appeal was received on 25 November 2008.

The examining division took its decision on the basis of the file as amended with the amendments filed on 18 June 2008, as requested by the applicant in his letter dated 7 July 2008.

The examining division held that the application did not meet the requirements of Articles 123(2), 84 EPC and did not involve an inventive step in the sense of article 56 EPC having regard to the documents:

D1 = K. Yamashita & al. "Frequency Stabilizing Method Using PSCL (phase slip-controlled loop)" 39th IEEE Vehicular Technology Conference, San Francisco, 1-3 May 1989, vol. 1, pages 215 to 219;

D3 = "A New Approach to Fractional-N Synthesis", Electronic Engineering, Woolwich, London, GB, vol. 62, March 1990, no.759, pages 35, 36 and 38; and

D4 = US-A-5038117.

II. In a communication dated 21 May 2012, accompanying a summons to oral proceedings, the board cited a new document D6 = GB-A-2 024 546 and questioned whether the subject-matter of the independent claims, then on file involved an inventive step having regard to the

combination of documents D1 and D4 or D6 and D4. Furthermore, the board considered in that communication that the expression "noise-shaping digital modulator" might be unclear.

III. In a reply dated 21 September 2012, the appellant filed a new main request and three auxiliary requests and referred to the following documents:
Exhibit 1: "A Low Area, Switched-Resistor Based Fractional-N Synthesizer Applied to a MEMS-Based Programmable Oscillator" by M.H.Perrott & al. IEEE 2010;
Exhibit 2: "Market Research on MEMS Oscillators".

On 10 October 2012, the applicant submitted a "statement from Professor Paul Victor Brennan commenting on the prior art documents (particularly D6)".

IV. Oral proceedings before the board took place on 12 October 2012.

V. The appellant requested that the decision under appeal be set aside and that the case be remitted to the department of first instance for further prosecution on the basis of claims 1 to 8 of a main request or claims 1 to 5 of an auxiliary request, both filed during the oral proceedings of 12 October 2012.

VI. Claim 1 of the main request reads as follows:

"A frequency synthesizer with temperature compensation and frequency multiplication, comprising:
a temperature dependent frequency oscillator (202);

at least one locked loop circuit (206) coupled to the oscillator (202) and chosen from the group consisting of a phase locked loop and a frequency locked loop;
at least one frequency division element (208, 222) in or coupled to the locked loop circuit, the element programmed to vary as a function of a temperature variation of the frequency oscillator (202) and to vary as a function of a frequency multiplication factor, wherein the at least one frequency division element is a multi-modulus divider;
a control circuit (210) including a temperature sensor (226) coupled to a temperature compensation controller (228), the controller is configured to provide a temperature-dependent modulator control signal based on a temperature measured by the temperature sensor;
a noise-shaping digital modulator (214) connected to the control circuit and the at least one division element (208, 222), the noise-shaping digital modulator in a control signal path of the control circuit (210) and responsive to the temperature-dependent modulator control signal provided by the controller to generate a temperature dependent divider control input to the at least one division element, the noise-shaping digital modulator being configured to vary the modulus of the at least one division element as a function of temperature by varying the temperature dependent divider control input so as to temperature compensate the frequency oscillator, wherein the noise-shaping digital modulator is configured to create an average divider modulus by varying the modulus in such a manner as to shape noise created as the modulus is varied; and
the oscillator (202), noise-shaping digital modulator (214) and the at least one division element (208, 222) being coupled such that a temperature independent

multiplied frequency synthesizer output (238) is provided."

Claims 2 to 7 are dependent on claim 1.

Claim 8 of the main request reads as follows:

"A method of temperature compensating and multiplying a frequency output in a frequency synthesizer, comprising the steps of:
providing (302) a temperature dependent frequency oscillator coupled to
at least one frequency division element being programmed to vary as a function of a temperature variation of the frequency oscillator and to vary as a function of a frequency multiplication factor, the frequency division element being connected to a noise-shaping digital modulator and being in or coupled to at least one locked loop circuit selected from the group consisting of a phase locked loop, and a frequency locked loop, wherein the frequency division element is a multi-modulus divider, wherein the noise-shaping digital modulator is configured to create an average divider modulus by varying the modulus in such a manner as to shape noise created as the modulus is varied;
measuring (304) an ambient temperature value in proximity to the oscillator;
searching (306) a lookup table for a predetermined temperature dependent modulator control signal corresponding to the ambient temperature value and the frequency multiplication factor; and
applying (308) the modulator control signal to the noise-shaping digital modulator to generate a temperature dependent divider control applied to the at

least one frequency division element, the temperature dependent divider control varying the modulus of the at least one division element as a function of temperature such that a desired temperature compensated and multiplied output frequency is obtained from the synthesizer."

VII. Claim 1 of the auxiliary request reads as follows:

"A frequency synthesizer with temperature compensation and frequency multiplication, comprising:
a temperature dependent frequency oscillator (202);
at least one locked loop circuit (206) coupled to the oscillator (202) and chosen from the group consisting of a phase locked loop and a frequency locked loop;
at least one frequency division element (208, 222) in or coupled to the locked loop circuit, the element programmed to vary as a function of a temperature variation of the frequency oscillator (202) and to vary as a function of a frequency multiplication factor, wherein the at least one frequency division element is a multi-modulus divider;
a control circuit (210) including a temperature sensor (226) coupled to a temperature compensation controller (228), the controller is configured to provide a temperature-dependent modulator control signal based on a temperature measured by the temperature sensor;
a noise-shaping digital modulator (214) connected to the control circuit and the at least one division element (208, 222), the noise-shaping digital modulator in a control signal path of the control circuit (210) and responsive to the temperature-dependent modulator control signal provided by the controller to generate a temperature dependent divider control input to the at

least one frequency division element, the noise-shaping digital modulator being configured to vary the modulus of the at least one division element as a function of temperature by varying the temperature dependent divider control input so as to temperature compensate the frequency oscillator wherein the noise-shaping digital modulator is configured to create an average divider modulus by varying the modulus in such a manner as to shape noise created as the modulus is varied; the oscillator (202), noise-shaping digital modulator (214) and the at least one division element (208, 222) being coupled such that a temperature independent multiplied frequency synthesizer output (238) is provided; and
at least one mixer (244), the at least one mixer (244) being coupled to a feedback path (240) of the loop circuit (206), and wherein the at least one frequency division element (222) is connected in an electrical path selected from one of the group of at least one signal path between the oscillator and the at least one mixer, and the at least one signal path between the oscillator and the loop circuit (206)".

Claims 2 to 4 are dependent on claim 1.

Claim 5 of the auxiliary request reads as follows:

"A method of temperature compensating and multiplying a frequency output in a frequency synthesizer, comprising the steps of:
providing (302) a temperature dependent frequency oscillator (202) coupled to at least one frequency division element (208, 222) being programmed to vary as a function of a temperature variation of the frequency

oscillator and to vary as a function of a frequency multiplication factor, the frequency division element being connected to a noise-shaping digital modulator (214) and being in or coupled to at least one locked loop circuit (206) selected from the group consisting of a phase locked loop, and a frequency locked loop, wherein the frequency division element is a multi-modulus divider wherein the noise-shaping digital modulator is configured to create an average divider modulus by varying the modulus in such a manner as to shape noise created as the modulus is varied;
providing at least one mixer (244), the at least one mixer (244) being coupled to a feedback path (240) of the loop circuit (206), and wherein the at least one frequency division element (222) is connected in an electrical path selected from one of the group of at least one signal path between the oscillator and the at least one mixer, and the at least one signal path between the oscillator and the loop circuit (206);
measuring (304) an ambient temperature value in proximity to the oscillator;
searching (306) a lookup table for a predetermined temperature dependent modulator control signal corresponding to the ambient temperature value and the frequency multiplication factor; and
applying (308) the modulator control signal to the noise-shaping digital modulator to generate a temperature dependent divider control applied to the at least one frequency division element, the temperature dependent divider control varying the modulus of the at least one division element as a function of temperature such that a desired temperature compensated and multiplied output frequency is obtained from the synthesizer."

VIII. The appellant essentially argued as follows:

Professor Paul Victor Brennan summarised the problem to be solved by the invention as follows: "The overall objective of the claimed arrangement is to provide compensation for the temperature-dependent frequency drift of the oscillator (such as that used in a mobile device) by means of the adjustment of the division ratio of the associated frequency synthesizer rather than by adjustment of the operating frequency of the oscillator itself."
Professor Paul Victor Brennan acknowledged that D1 did solve this problem but confirmed that the present invention differed from D1 and D4, as well as from D6.

D1 gave little information and there were doubt that the circuit of D1 would work due to spurious effects and a loop filter which would need to be adapted. D1 proposed to send a correction value of the phase slip to the loop filter over a digital-analog converter. This solution could not be accurate. The adaptation rate of the division factor of D1, once per cycle time, was much slower than the adaptation rate of a fractional divider.

D4 did not refer at all to any temperature compensation.

Starting from D4, a man skilled in the art willing to compensate the temperature dependent frequency drift would apply the well-known, existing solutions and would correct the oscillator output. D4 was a balanced system which involved a zero mean modulation. Changing

the values of the fractional divider would unbalance the circuit of D4. A person of ordinary skill would therefore not be tempted to modify the circuit of D4. Reading out of D1 a teaching to modify the frequency divider would amount to ex-post isolating a feature. The serial data signal of D1 were applied to an element called frequency divider in figure 1, but the document as a whole was unclear about the effect of the serial data. A person of ordinary skill would not apply the teachings of D1 to D4, because he would not know how to apply the serial data to the phase lock loop frequency divider of D4.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

The objections raised by the examining division against the independent claims of the request filed on 18 June 2008 that related to Articles 123(2) and 84 EPC have been overcome as follows:

2.1 The "frequency multiplication element" corresponding to the multi-modulus divider 222 of the embodiments of the invention shown in figures 6 to 9 has been renamed "frequency division element" as suggested by the examining division. It has been further specified by the added feature "wherein the at least one frequency division element is a multi-modulus divider" based on original page 10, lines 15 and 16.

2.2 The objected term "modulus" in the feature "temperature dependent divider modulus control input" has been deleted and the following feature based on the passage found at page 11, lines 12 to 18 introduced: "the noise-shaping digital modulator...responsive to the temperature-dependent modulator control signal provided by the controller to generate a temperature dependent divider control input to the at least one division element". The omission of the term "modulus" from the original expression "temperature dependent divider modulus control signal" is accepted because the modulator does not generate a modulus but a control input for varying the modulus.

2.3 In combination with a multi-modulus divider generating an average divider modulus, the expression "noise-shaping digital modulator" appears to be clear because it is a common practice to control a multi-modulus divider by a modulator, e.g. a delta-sigma modulator, in a way to reject the noise. In the independent claims of the main and auxiliary requests, the expression "noise-shaping digital modulator" has been further clarified in functional terms: "the noise-shaping digital modulator is configured to create an average divider modulus by varying the divider modulus in such a manner as to shape the noise created as the modulus is varied". Support for this definition can be found in the original description at page 12, lines 21 to 25.

2.4 The feature "the frequency multiplication element having a noise-shaping digital modulator in or coupled to at least one lock loop circuit" has been reformulated as "the frequency division element being connected to a noise-shaping digital modulator and

being in or coupled to at least one locked loop circuit", whereby the noise-shaping digital modulator is not anymore part of the loop circuit as objected by the examining division as infringing Article 123(2) EPC.

Thus, the amendments to the application do not contravene Article 123(2) EPC and are considered as clarifying the subject-matter of the claims.

3. *Novelty*

Among the different documents cited during the procedure before the first instance, solely D1 provides temperature compensation for a frequency synthesizer.

D1 discloses a "frequency synthesizer" with a division factor controlled on the basis of a serial data signal. The serial data comprise three factors: M, N and P, representing respectively the main counter division factor, the swallow counter value and a factor (P) representing the temperature dependent frequency variations. P is received by a "phase slip-controlling signal generator" which, on the one hand, acts on a digital/analog converter (D/A) to generate a voltage compensating the phase slip caused by the cyclic change of the division ratio (cf. page 215, right-hand column, last paragraph), and, on the other hand, acts onto the swallow counter to raise the division ratio of a dual-modulus prescaler by a factor of two.
The swallow counter, the dual-modulus prescaler and the main counter divide the output frequency successively N times by a factor of 66 and M-N times by a factor of 64. The resulting division factor m' is as represented on figure 4:

m' = 64(M-N) + 66N = 64M + 2N = 26M + 2N.
The 8 bits of the M factor correspond to D18 to D25 while D12 to D17 correspond to the factor N. Each bit D0 to D11 (factor P) represents the necessary frequency correction which can vary between 50Hz and 100kHz (cf. figure 3). D0 to D11 define a number of cycles with a division ratio m' before the factor m' is raised by a factor of 2 during one cycle. This is controlled by the swallow counter value changing from N to N+1 (cf. the value "+1" in figure 2). The effect when D8 or D9 is equal to 1 is shown in figures 4a and 4b. The resulting division factor m is as recited in the left hand column of page 216:
m = 26xM + 2xN + 2-11xP.
Simultaneously the temperature compensation voltage is applied to the loop filter over the digital/analog converter to compensate the phase slip caused by a cyclic change of the division ratio (cf. page 215, right-hand column, last paragraph).

The frequency divider of D1 may thus be seen as a very particular fractional frequency divider with a frequency output depending on the temperature variations. However the frequency incremental step is determined by the number of bits D0 to D25 of the serial data and the main frequency allocated to the bit D25 (cf. page 216, right hand column, last paragraph in combination with figure 3). The step value is independent of the temperature variations.

Hence it can be considered that D1 discloses a frequency synthesizer with temperature compensation and frequency multiplication (cf. figure 1) comprising:

a temperature dependent frequency oscillator (xtal osc & thermosensor) (cf. figure 1);
at least one locked loop circuit coupled to the oscillator and chosen from the group consisting of a phase locked loop (PSCL, fig.1) and a frequency locked loop;
at least one frequency division element (frequency divider) in or coupled to the locked loop circuit, the element programmed to vary as a function of a temperature variation of the frequency oscillator and to vary as a function of a frequency multiplication factor, wherein the at least one frequency division element is a multi-modulus divider (the dual-modulus prescaler); and
a control circuit (CPU and data rom) including a temperature sensor (thermo-sensor) coupled to a temperature compensation controller (the CPU), the controller being configured to provide a temperature-dependent control signal (the serial data D0-D25) based on a temperature measured by the temperature sensor.

The control signal applies the serial data to a frequency divider. The serial data raise the frequency divider ratio by a factor of two at the end of a predetermined number of division cycles. However it is not unambiguously derivable from D1 that the frequency divider would be controlled "so as to create an average divider modulus by varying the modulus in such a manner as to shape noise created as the modulus is varied". It follows that D1 does not comprise a noise-shaping modulator as claimed.
The subject-matter of claims 1 to 8 of the main request, respectively claims 1 to 5 of the auxiliary request is therefore new (Article 54 EPC).

4. *Inventive step*

A frequency synthesizer comprising a noise-shaping modulator is disclosed in D4 which can be regarded as a suitable starting point for assessing inventive step.

4.1 D4 discloses "a frequency synthesizer with frequency multiplication, comprising:
a frequency oscillator (input to the phase comparator 15);
at least one phase locked loop circuit (cf. column 4, lines 35 to 40) coupled to the oscillator;
at least one frequency division element 13 (cf. column 4, lines 41 to 42) in or coupled to the locked loop circuit, the element programmed to vary as a function of a frequency multiplication factor, wherein the at least one frequency division element is a multi-modulus divider (cf. column 5, lines 21 to 29);
Figure 8 shows a detailed block diagram of the multiple modulus fractional divider 13. It comprises a noise-shaping digital modulator in a control signal path of a control circuit 18, connected to the control circuit 18 and to the division element 53. The noise-shaping digital modulator is configured to create an average divider modulus by varying the modulus in such a manner as to shape noise created as the modulus is varied (cf. column 10, line 52 to column 11, line 26).

4.2 The subject-matter of claim 1 of the main request differs from D4 in that:
the control circuit includes a temperature sensor coupled to a temperature compensation controller, the controller being configured to provide a temperature-

dependent modulator control signal based on a temperature measured by the temperature sensor,

the noise-shaping digital modulator is responsive to the temperature-dependent modulator control signal provided by the controller to generate a temperature dependent divider control input to the at least one division element,

the noise-shaping digital modulator is configured to vary the modulus of the at least one division element as a function of temperature by varying the temperature dependent divider control input so as to temperature compensate the frequency oscillator,

the oscillator, noise-shaping digital modulator and the at least one division element being coupled such that a temperature independent multiplied frequency synthesizer output is provided.

4.3 The problem to be solved may be seen in stabilizing the frequency with respect to temperature variations. A solution to this problem is proposed in D1.

4.4 To compensate for temperature variations, D1 teaches to apply a correction factor to the swallow counter after a predetermined number of division cycles. The swallow counter and the prescaler of D1 are part of the frequency divider.

4.5 D1 is silent about the effects of switching the dividing ratio from m' to m'+2 after a predetermined number of cycles. It is however unlikely that the noise created thereby would be shaped. Furthermore, D1

applies a correcting voltage value issued by the digital/analog converter to the loop filter, which might reduce the noise.

The application of the teaching of D1 to a fractional divider as shown in D4 might lead to increase, respectively decrease one of the two or more divider moduli of the multi-modulus fractional divider of D4 by a factor of two after a predetermined number of cycles. However, as in D1, this step might not lead to a frequency increase, respectively decrease, in the range of the frequency drift caused by the temperature variations. Furthermore, a fractional divider according to the embodiments shown in figures 8 and 11 to 12 of D4 switches between at least two moduli and rejects the noise outside the central frequency band (cf. figure 12). Raising one of the modulus by a factor of two according to the teaching of D1 after a predetermined number of cycles could interfere with the shaping of the noise created as the modulus is varied, because it would unbalance the circuit of D4.

4.6 As a correction of the division factor as taught in D1 cannot be applied directly to the modulus of D4, the notional uninventive skilled person would not know where to apply the divider correction value issued by the thermo-sensor over the phase slip-controlling signal generator. Thus, the skilled person would not combine D1 and D4.

4.7 D3 discloses a frequency synthesizer comprising a multi-modulus divider similar to the one disclosed in D4. For the same reasons as above, it would not be obvious to combine the teachings of D1 and D3.

5. As indicated in the communication of the board attached to the summons to oral proceedings, the newly cited document D6 presents some similarities with the claimed subject-matter and appears to be relevant for the assessment of inventive step. Moreover, substantial amendments have been made to the claims and the appellant has explicitly asked for a remittal to the first instance. In these circumstances the board, making use of its power under Article 111(1) EPC, finds it appropriate to remit the case to the examining division for further prosecution in order to give to the appellant the opportunity to defend their claims before two instances.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu