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Datasheet for the decision of 24 February 2014

Case Number: T 0006/09 - 3.5.02

Application Number: 01000689.8

Publication Number: 1217745

IPC: H03L7/107

Language of the proceedings: EN

Title of invention:
Digital PLL with adjustable gain

Applicant:
Texas Instruments Incorporated

Headword:

Relevant legal provisions:
EPC Art. 84, 123(2), 54, 56

Keyword:
Claims - clarity after amendment (yes)
Amendments - extension beyond the content of the application as filed (no)
Novelty - (yes)
Inventive step - (yes)

Decisions cited:

Catchword:

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Case Number: T 0006/09 - 3.5.02

D E C I S I O N
of Technical Board of Appeal 3.5.02
of 24 February 2014

Appellant: (Applicant)	Texas Instruments Incorporated 7839 Churchill Way Mail Station 3999 Dallas, Texas 75251 (US)
Representative:	Holt, Michael Texas Instruments Limited European Patent Department 3rd Floor 401 Grafton Gate Milton Keynes MK9 1AQ (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 11 July 2008 refusing European patent application No. 01000689.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman: M. Ruggiu
Members: M. Léouffre
P. Mühlens

Summary of Facts and Submissions

I. The applicant lodged an appeal, received on 12 August 2008, against the decision of the examining division, dated 11 July 2008, to refuse European patent application No. 01000689.8. The decision under appeal was based on the following application documents:
Description: pages 1, 3 and 5 to 9 as originally filed; pages 2a and 10 filed with letter of 15 August 2006; pages 2 and 4 filed with letter of 2 June 2008.
Claims: No. 1 to 7 filed during oral proceedings of 1 July 2008.
Drawings: sheets 1/2 and 2/2 as originally filed.

II. The examining division held that claim 1 of the application did not meet the requirements of Article 84 EPC and indicated that in their view the subject-matter of claims 1, 2, 3 and 6 was not new (Article 54 EPC), having regard to document
D1 = US 6 018 556 A.

III. With the statement setting out the grounds of appeal, received on 11 November 2008, the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of a new main request and a new auxiliary request appended thereto.

IV. In an annex to summons to oral proceedings, dated 27 November 2012, the board expressed the preliminary opinion that the independent claims of both requests were not clear (Article 84 EPC) and contained subject-matter which extended beyond the content of the application as filed, contrary to Article 123(2) EPC.

V. The appellant reacted with a fax dated 7 January 2013 requesting the grant of a patent on the basis of a new main request which fulfilled the requirements following from Article 123(2) EPC and wherein the major clarity objections were remedied.

VI. Following a telephone conversation between the rapporteur and the appellant, the latter, on 19 February 2014, filed a complete new description, set of claims and drawings.

VII. Claim 1 reads as follows:

"A method of adjusting a loop gain constant in a phase-lock loop (PLL) synthesizer (100) having a controllable oscillator (108) that is controlled by an oscillator-tuning signal (107) and wherein a phase error Φ in the PLL synthesizer, after phase/frequency acquisition, is proportional to frequency offset in said controllable oscillator (108), said method comprising:

(a) using a first PLL loop gain constant α_1 during a phase/frequency acquisition mode of the PLL synthesizer;

(b) performing the following two steps when the PLL synthesizer transitions from the phase/frequency acquisition mode into a tracking mode:

(b1) adding a DC offset to the oscillator-tuning signal; and

(b2) changing the first PLL loop gain constant α_1 to a second PLL loop gain constant α_2 which is smaller in value than the first PLL loop gain constant α_1,

whereby the DC offset adjusts the phase error Φ for the change to second PLL loop gain constant α_2 by a phase error adjustment $\Delta\Phi$ such that there is no resultant frequency perturbation of the controllable oscillator

(108) from before said transition of the PLL synthesizer (100) to after said transition of the PLL synthesizer (100); and
(c) maintaining said phase error adjustment $\Delta\Phi$ constant during said tracking mode of said PLL synthesizer."

Claims 2 to 5 are dependent on claim 1.

Claim 6 reads as follows:

"A PLL synthesizer (100) having a controllable oscillator (108) that is controlled by an oscillator-tuning signal (107) and wherein a phase error Φ in the PLL synthesizer, after phase/frequency acquisition, is proportional to a frequency offset in said controllable oscillator (108), comprising:
circuitry for using a first PLL loop gain constant α_1 during a phase/frequency acquisition mode of the PLL synthesizer; and characterised by
circuitry for adding and maintaining constant a DC offset to the oscillator-tuning signal and for changing the first PLL loop gain constant α_1 to a second loop gain constant α_2 which is smaller in value than the first PLL loop gain constant α_1 when the PLL synthesizer transitions from the phase/frequency acquisition mode into a tracking mode,
whereby the DC offset adjusts the phase error Φ for the change to the second PLL loop gain constant α_2 by a phase error adjustment amount $\Delta\Phi$ such that there is no resultant frequency perturbation of the controllable oscillator (108) from before said transition of the PLL synthesizer (100) to after said transition of the PLL synthesizer (100)."

Claim 7 is dependent on claim 6.

VIII. The appellant essentially argued in writing as follows:
The claims had been clarified and aligned with the description.
The claims did not restrict normal PLL operation to acquire a frequency, to react to a frequency hop at the input (i.e. acquire a new frequency) or track a frequency. These frequency perturbations still occurred and were not inconsistent with the claims.
The applicant was of the view that claim 1 defined an invention in which the loop gain of a PLL might be changed from a relatively high value (acquisition mode) to a relatively lower value (tracking mode) without the frequency perturbation to the loop output from before the change to after the change by providing a DC offset added to the control of the loop oscillator when the change was made.
It was not apparent that in D1 a frequency stabilising DC offset was added when the PLL transitioned from the acquisition mode to the tracking mode.

Reasons for the Decision

1. Article 123(2) EPC

1.1 Claim 1 is based on original claim 1 and adds the following features:

a) a controllable oscillator (108) "that is controlled by an oscillator-tuning signal (107) and wherein a phase error Φ in the PLL synthesizer, after phase/frequency acquisition, is proportional to frequency offset in said controllable oscillator (108)"; and

b) "whereby the DC offset adjusts the phase error Φ for the change to second PLL loop gain constant α_2 by a phase error adjustment $\Delta\Phi$ such that there is no resultant frequency perturbation of the controllable oscillator (108) from before said transition of the PLL synthesizer (100) to after said transition of the PLL synthesizer (100)"; and

c) "maintaining said phase error adjustment $\Delta\Phi$ constant during said tracking mode of said PLL synthesizer."

1.2 Feature a) limits the protection conferred by claim 1 to PLL synthesizer of type I. This is in line with the original description as recited in the summary of invention at page 2, lines 13 to 25 and in the detailed description of the preferred embodiment in the sentence bridging pages 3 and 4 of the application as filed. Feature b) defines the DC offset and the phase error adjustment by their functions with respect to a transition from acquisition mode to tracking mode. There is no explicit mention of these definitions in the original description. However the original description at page 2, lines 17 to 23 discloses that, while transitioning into the tracking mode, the addition of a DC offset to the VCO tuning signal "results in substantial lowering of maximum phase error" whereby α (the loop gain) can then be safely reduced from α_1 to α_2. Hence the original application discloses the feature of claim 1 that "the DC offset adjusts the phase error Φ for the change to second PLL loop gain constant α_2 by a phase error adjustment $\Delta\Phi$". The original description at page 5, lines 16 to 21 recites that "the new phase error value $\Phi_2 = \Phi_1 + \Delta\Phi$ is adjusted for the new lower tracking-mode loop gain value α_2 114 such that there is no frequency perturbation of the oscillator 108 before and after the

event" i.e before and after the transition from acquisition mode to tracking mode of the PLL synthesizer. In its literal meaning, this original expression is erroneous because an event cannot influence the frequency perturbations having occurred before the event. Hence, in the light of figures 3 and 4, a person skilled in the art would have immediately understood that this original expression was intended to mean that a transition from acquisition mode to tracking mode would not result in adding frequency perturbations. The board considers therefore that the feature "no resultant frequency perturbation of the controllable oscillator (108) from before said transition of the PLL synthesizer (100) to after said transition of the PLL synthesizer (100)" does not infringe Article 123(2) EPC.
Finally feature c) is disclosed in the original application wherein the phase error adjustment value is said to be maintained constant throughout the tracking mode operation (cf. original description at page 6, lines 1 to 4).

1.3 Thus, claim 1 and claim 6, which comprises only apparatus features corresponding to the features of method claim 1, comply with the requirements following from Article 123(2) EPC.
Dependent claims 2 to 5 are supported by the original dependent claims 2, 12, 3 and 6, while the features of dependent claim 7 are disclosed in original claim 13 and figure 1. The dependent claims do therefore also comply with the requirements following from Article 123(2) EPC.

2. Article 84 EPC

2.1 The examining division referred to Guidelines C-III-4.1 and 4.2 and held that the meaning of the terms used in a claim should be clear to a person skilled in the art from the wording of the claim alone. The examining division considered the following expressions as unclear:

(a) the expression "when the PLL synthesizer transitions" was ambiguous (moment or period);

(b) the expressions "a phase error Φ" and "an uncorrected phase error signal Φ" might not refer to the same feature;

(c) "said control" would be unclear since there was no antecedent;

(d) it would be unclear how the second loop gain constant α_2 is to be changed, the change being from α_1 to α_2;

(e) "a DC offset in said control" would be unclear;

(f) it was unclear how "no frequency perturbation of the controllable oscillator before and after said transition" is achieved, since Fig. 4, shows frequency perturbations before the transition.

2.2 Objection (a) was remedied by defining the DC offset and specifying that the DC offset is maintained constant during the tracking mode.
Objections (b), (c) and (e) were remedied by removing the expressions "uncorrected phase error signal," "said control" and "a DC offset in said control".
Objection (d) did not apply since the independent claims of the contested decision did not consider any change of the value of the second loop gain constant α_2.
Objection (f): see item 1.2 above.

2.3 With the new claims 1 and 6, the appellant has therefore remedied the clarity objections raised by the examining division.

3. Articles 54 and 56 EPC

3.1 The examining division considered D1 as representing the closest prior art. According to the examining division the output of the integrator 203 of the loop filter 166 shown in figure 2 of D1 would produce a DC offset (cf. item 5.1 of the contested decision), and the application would at most differ from D1 in that "the steady DC offset is not added during phase/ frequency acquisition mode" (cf. item 5.2 of the contested decision).

3.2 Claims 1 and 6 now specify that when the PLL synthesizer transitions from the phase/frequency acquisition mode into the tracking mode, the DC offset is added and maintained constant during the tracking mode. It should be understood therefrom that, indeed, a DC offset is not added during phase/frequency acquisition mode contrary to the PLL of D1. Furthermore, the subject-matter of claims 1 and 6 differs from the PLL according to D1 in that a constant DC signal, i.e. a constant DC offset, is added during the tracking mode, contrary to the inherently variable integrator output signal of the loop filter 166 shown in D1. Claims 1 and 6 are therefore novel having regard to D1 (Article 54 EPC).

3.3 Starting from document D1 and considering document D1 alone, adding a constant DC offset to the oscillator-tuning signal at the time of transition from acquisition mode to tracking mode in order to avoid introducing frequency perturbations from before said transition of the PLL synthesizer to after the transition of the PLL synthesizer is not obvious (Article 56 EPC).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   Description:
   Pages 1, 2, 2a and 3 to 10 filed with letter dated 19 February 2014.

   Claims:
   No. 1 to 7 filed with letter dated 19 February 2014.

   Drawings.
   Sheets 1/2 and 2/2 filed with letter dated 19 February 2014.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu

Decision electronically authenticated