Internal distribution code:

(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 30 January 2013

Case Number: T 2280/08 - 3.5.04

Application Number: 06001264.8

Publication Number: 1763039

IPC: G11C16/34

Language of the proceedings: EN

Title of invention:
Method and apparatus for protection from over-erasing nonvolatile memory cells

Applicant:
MACRONIX INTERNATIONAL CO., LTD.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56, 111(1)
RPBA Art. 13(1)

Keyword:
Inventive step - (no)
Decision re appeals - remittal (yes)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 2280/08 - 3.5.04

D E C I S I O N
of the Technical Board of Appeal 3.5.04
of 30 January 2013

Appellant: (Applicant)	MACRONIX INTERNATIONAL CO., LTD. No.16, Li-Hsin Road, Science-Based Industrial Park Hsinchu (TW)
Representative:	Buchhold, Jürgen Patentanwälte Olbricht Buchhold Keulertz Partnerschaft Bettinastraße 53-55 60325 Frankfurt am Main (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted 18 July 2008 refusing European patent application No. 06001264.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman: F. Edlinger
Members: C. Kunzelmann
C. Vallet

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 06 001 264.8 under Article 97(2) of the European Patent Convention (EPC).

II. The application was refused on the ground that the method of claim 1 did not involve an inventive step (Article 56 EPC) having regard to the state of the art disclosed in

D1: US 2005/0073886 A1 and
D2: EP 1 555 674 A1

and that the subject-matter of claims 12 and 23 did not involve an inventive step having regard to the state of the art disclosed in D2 (see above) and

D3: US 5 930 174 A.

III. Claim 1 reads as follows:

"A method for erasing charge trapping memory cells, comprising:
in response to a command to erase a plurality of charge trapping memory cells each having a charge trapping structure associated with a threshold voltage, a programmed state, and an erased state:
applying a first bias arrangement to program charge trapping memory cells in the plurality of charge trapping memory cells;
and then
applying a second bias arrangement to establish the erased state (620) in the plurality of charge trapping memory cells, wherein the charge trapping structure of

each charge trapping memory cell of the plurality of charge trapping memory cells has a higher net electron charge in the erased state (620) than in the programmed state (610, 615, 625)."

Claim 23 reads as follows:

"A method of manufacturing a charge-trapping integrated circuit, comprising:
making an array of charge-trapping memory cells each having a charge trapping structure associated with a threshold voltage and a programmed state and an erased state;
and
coupling logic to the array, said logic responsive to a command to erase a plurality of charge trapping memory cells in the array by performing:
applying a first bias arrangement to program charge trapping memory cells in the plurality of charge trapping memory cells having the threshold voltage outside the programmed state; and then
applying a second bias arrangement to establish the erased state in the plurality of charge trapping memory cells, wherein the charge trapping structure of each charge trapping memory cell of the plurality of charge trapping memory cells has a higher net electron charge in the erased state than in the programmed state."

IV. With the statement of grounds of appeal, the appellant filed claims 1 to 21 according to a first auxiliary request. Claim 21 of the first auxiliary request is identical to claim 23 of the main request.

V. The board issued a communication pursuant to Article 15(1) of the Rules of Procedure of the Boards of Appeal (RPBA), annexed to a summons to oral

proceedings. The board indicated that it tended to agree with the finding in the decision under appeal that the method according to claim 1 of the main request lacked an inventive step having regard to D1 and D2. The board also indicated that it envisaged remitting the case to the department of first instance on the basis of the first auxiliary request if it came to the conclusion that the appellant's main request could not be allowed.

VI. Oral proceedings before the board were held on 30 January 2013. During the oral proceedings the appellant filed claims 1 to 20 according to a second auxiliary request. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims of the main request or, in the alternative, on the basis of claims 1 to 21 of the first auxiliary request, filed with the statement of grounds of appeal, or, in the alternative, on the basis of claims 1 to 20 submitted in the oral proceedings before the board. At the end of the oral proceedings, the chairman announced the board's decision.

VII. Claim 1 of the second auxiliary request reads as follows:

"A method for erasing charge trapping memory cells, comprising:
in response to a command to erase a plurality of charge trapping memory cells each having a charge trapping structure associated with a threshold voltage, a programmed state, and an erased state:
applying a first bias arrangement to program charge trapping memory cells in the plurality of charge trapping memory cells; and then

applying a second bias arrangement to establish the erased state (620, 630) in the plurality of charge trapping memory cells,
wherein the charge trapping structure of each charge trapping memory cell of the plurality of charge trapping memory cells has a higher net electron charge in the erased state (620, 630) than in the programmed state (610, 615, 625), and
wherein the charge trapping structure of each charge trapping memory cell in the plurality of charge trapping memory cells has a first charge trapping part and a second charge trapping part, each of the first charge trapping part and the second charge trapping part associated with a threshold voltage and an erased state and a plurality of programmed states, the plurality of programmed states including a most programmed state and a subplurality of less programmed states,
said applying the first bias arrangement includes applying the first bias arrangement to program any said first charge trapping part and any said second charge trapping part having the threshold voltage in one of the erased state and any of the subplurality of less programmed states, and
said applying the second bias arrangement includes applying the second bias arrangement to establish the erased state in the first charge trapping part and the second charge trapping part of each charge trapping memory cell in the plurality of charge trapping memory cells."

Amendments with respect to claim 1 of the main request are set in *italics*.

VIII. The reasons for the decision under appeal may be summarised as follows:

D1 disclosed a method for erasing charge trapping memory cells having all the steps specified in claim 1, but resulting in a lower net electron charge in the charge trapping layer in the erased state than in the programmed state. D1 solved the problem of over-erasure of memory cells by applying a pre-programming step prior to applying the erasing step. Memory cells having a charge trapping structure which had a higher net electron charge in the erased state than in the programmed state were known from D2. Since the memory cells of D1 and D2 had the same structure, a person skilled in the art would expect the problem of over-erasure of memory cells to occur also in the memory cells of D2 and would adopt the solution known from D1, namely applying a pre-programming step prior to applying the erasing step. The pre-programming step would be carried out using the normal programming method in D2, namely hole injection, and the erasing step would be carried out using electron injection, thereby increasing the net electron charge in the erased state. Thus the method of claim 1 did not involve an inventive step.

Independent claims 12 and 23 added the further feature that a selection step was provided wherein the first bias arrangement was applied only to unprogrammed memory cells. This feature was known from D3 and had also the advantage of reducing over-erasure of memory cells. Hence also the subject-matter of claims 12 and 23 did not involve an inventive step.

The decision under appeal also comprised a statement that the subject-matter of dependent claims 6 and 17 was considered to meet the requirements of novelty and inventive step.

IX. The appellant's arguments may be summarised as follows:

The decision was based on hindsight. If a citation taught a higher net electron charge, a person skilled in the art would not come to a solution which meant the contrary. If D1 was considered as the closest prior art, then the objective problem in the context of the problem-and-solution approach should have been formulated in view of D1. Since D1 solved the problem of over-erasure of memory cells, the problem to be solved could not be that of avoiding over-erasure. Instead the objective problem would have been to avoid leakage current of the memory cell. Since neither D1 nor D2 solved this problem, the method of claim 1 involved an inventive step.
D2 had been indirectly considered in the present application because figures 4A and 4B of D2 corresponded to figures 1A and 1B of the present application. If D2 was taken as the closest prior art, then the problem solved was that of performing an erase operation on a non-volatile memory cell while reducing the tendency of the distribution of threshold voltages of non-volatile memory cells in the erased state to drift if program-and-erase cycles occurred repeatedly. This drift was avoided by pre-programming all the memory cells prior to erasing them. This problem of drifting threshold voltages was not solved by D1 or D2.

Reasons for the Decision

1. The appeal is admissible.

2. Main request: inventive step (Article 56 EPC 1973)

2.1 Claim 1

2.1.1 Figures 4A and 4B of D2 illustrate memory cells functioning according to the same operating principles as the prior art considered in figures 1A and 1B of the present application. The memory cells belong to a plurality of memory cells which may be erased together (see paragraphs [0003] and [0004]). According to D2 the memory cells (10) have a charge trapping structure (104 in Figure 2), a programmed state and an erased state. In the erased state, the trapping structure has a higher net electron charge than in the programmed state (see, for instance, paragraphs [0039], [0042] or [0047]). The erased state is reached by applying a bias arrangement (see, for instance, paragraphs [0047] or [0048]). In view of the similar structure and bias arrangements, the board considers D2 as a suitable starting point for assessing inventive step.

2.1.2 The method of erasing charge trapping memory cells according to claim 1 of the main request differs from the method disclosed in D2 in the feature of applying a first bias arrangement to program charge trapping memory cells in the plurality of charge trapping memory cells. This step is carried out prior to applying the bias arrangement to establish the erased state. One of the effects achieved thereby is disclosed in the application as avoiding "an undesirable wide distribution 430 of threshold voltages" occurring in the prior art (see paragraph [0006], last sentence, and paragraph [0029], last sentence, and figures 4C and 6C). The technical problem may thus be formulated as reducing the range of threshold voltage distributions in the erased state.

2.1.3 In the given context of charge trapping memory cells it was known that tighter threshold voltage distributions in the erased state were advantageous (see D1, the abstract, paragraphs [0008] and [0050] and figure 7). D1 discloses that such tighter threshold voltage distributions may be achieved by applying a pre-programming voltage, a gate stress and a soft programming voltage (see, for instance, figures 3 to 6 and paragraphs [0040] to [0048]).

2.1.4 Thus it would have been obvious to a person skilled in the art to apply a pre-programming voltage, a soft programming voltage and a gate stress of appropriate polarity as well as an erase voltage to the charge trapping memory cells of D2 in order to arrive at a tighter threshold voltage distribution in the erased state.

2.2 The appellant argued that the problem to be solved with respect to D2 was the one indicated in the description, paragraph [0007], namely "to perform an erase operation on a non-volatile memory cell while reducing the tendency of the distribution of threshold voltages of non-volatile memory cells in the erased state to drift." However, this tendency to drift is a subordinate or consequential problem occurring when program and erase cycles are carried out repeatedly (see paragraphs [0030] and [0031] and figures 7 and 8 of the application).

2.2.1 The appellant also argued that erasure of memory cells in D1 resulted in a lower electron density as opposed to the higher net electron charge specified in claim 1. However, the erasure and the programming of memory cells may be essentially opposite operations performed

by, for instance, electron injection and hole injection or vice versa. This is also described in the present application (see paragraph [0011]). In this respect the board agrees with the finding in point 9 of the decision under appeal that "threshold voltage drifts due to injection of electrons and/or holes and recombinations thereof are governed by the same physical principles ...". Thus a person skilled in the art would have applied appropriate pre-programming and erasure voltages both in respect of polarity and absolute values, as well as a gate stress and a soft programming voltage, in order to tighten the threshold voltage distribution of a plurality of charge trapping memory cells described in D2.

2.2.2 Also the appellant's argument that D1 did not solve the objective problem because it aimed at avoiding over-erasure of memory cells did not convince the board. D1 discloses two effects caused by applying a pre-programming voltage, a gate stress and a soft programming voltage, namely "correcting or otherwise compensating an array of overerased dual-bit memory cells" and "tighter threshold voltage distributions" (see paragraph [0045]). For the assessment of inventive step it does not matter which of the two effects is considered to be the main or the additional effect in the context of D1. Moreover, even though the term "over-erasure" is not used in the claims and description of the present application as filed, the step of applying a first bias arrangement to program charge trapping memory cells in the plurality of charge trapping memory cells prior to applying the erasure step may also avoid over-erasure of memory cells because this step may avoid erasure of already erased memory cells. Indeed, the title of the invention

is "Method and apparatus for protection from over-erasing nonvolatile memory cells".

2.3 In view of the above the board finds that the method of claim 1 according to the main request does not involve an inventive step (Article 56 EPC 1973).

2.4 Claim 23

2.4.1 The method of manufacturing a charge-trapping integrated circuit of claim 23 comprises the steps of "making an array of charge-trapping memory cells ..." and "coupling logic to the array ...". These steps are implicit in any method of manufacturing a charge-trapping integrated circuit. The further features essentially only specify features corresponding to the method of claim 1. In view of the disclosure in the present application these features do not relate to the manufacturing of the integrated circuit but instead to the erasing of memory cells when the manufactured integrated circuit is used. Moreover, the features corresponding to the method of claim 1 do not imply any steps in the manufacturing of the array, logic and bias arrangements cited in claim 23 which go beyond conventional manufacturing methods for manufacturing a charge-trapping integrated circuit comprising, in combination, an array of charge-trapping memory cells and logic coupled to the array, and bias arrangements. Furthermore, contrary to the opinion expressed in the decision under appeal, the board does not interpret claim 23 as comprising a selecting step wherein the first bias arrangement is applied only to unprogrammed memory cells. Thus the reasons given in the context of claim 1 also apply to the method of claim 23.

2.4.2 Thus the board finds that the method of claim 23 according to the main request does not involve an inventive step (Article 56 EPC 1973).

2.5 In view of the above the board finds that the decision to refuse the application was correct.

3. First auxiliary request: inventive step (Article 56 EPC 1973)

Claim 21 of the first auxiliary request is identical to claim 23 of the main request. Thus the first auxiliary request cannot be allowed for the reasons given in section 2.4 above.

4. Admission of the second auxiliary request (Article 13(1) RPBA)

The second auxiliary request may be considered as a reaction to objections of lack of clarity and inventive step raised for the first time by the board during the oral proceedings against the independent claim directed to a method of manufacturing a charge-trapping integrated circuit. After deleting this claim, the sole independent claims 1 and 11 correspond to independent claims 1 and 11 of the first auxiliary request with reference signs added and are, in substance, a combination of original claims 1 and 6 and 12 and 17, respectively. The decision under appeal stated in point 11 that the subject-matter of original dependent claims 6 and 17 met the requirements of novelty and inventive step. Thus the claims of the second auxiliary request reduce the complexity of the new subject-matter in a situation where the board had indicated its intention to remit the case to the first instance on the basis of such subject-matter. Hence the board

decided to exercise its discretion by admitting the claims according to the second auxiliary request into the appeal proceedings.

5. Remittal (Article 111(1) EPC 1973)

5.1 The board does not consider it appropriate to go beyond its primary task of examining the contested decision. In the present case, the brief indication given by the examining division with respect to original dependent claims 6 and 17 does not allow the conclusion that the current application documents are ready for the grant of a patent. In this context the board notes, for instance, that the description is not adapted to the present claims.

5.2 Moreover, the decision under appeal comprises in point 10 a statement that claims 12 and 23 then on file added the further feature that a selection step was provided wherein the first bias arrangement was applied **only** to unprogrammed memory cells. The board does not consider that this statement is correct (see point 2.4.1 above) in view of the present application documents and notes that according to dependent claims 3 and 13 the first bias arrangement programs **all** charge trapping memory cells in the plurality of charge trapping memory cells (emphasis by the board).

5.3 In view of the above the board decided to exercise its discretion by remitting the case to the department of first instance for further prosecution.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

K. Boelicke F. Edlinger

Decision electronically authenticated